AD-A077 572 TEXAS INSTRUMENTS INC DALLAS CENTRAL RESEARCH LABS F/G 9/5
BINARY/ANALOG CCD CORRELATOR DEVELOPMENT.(U)
SEP 79 R A HAKEN , R C PETTENGILL F19628-78-C-0122
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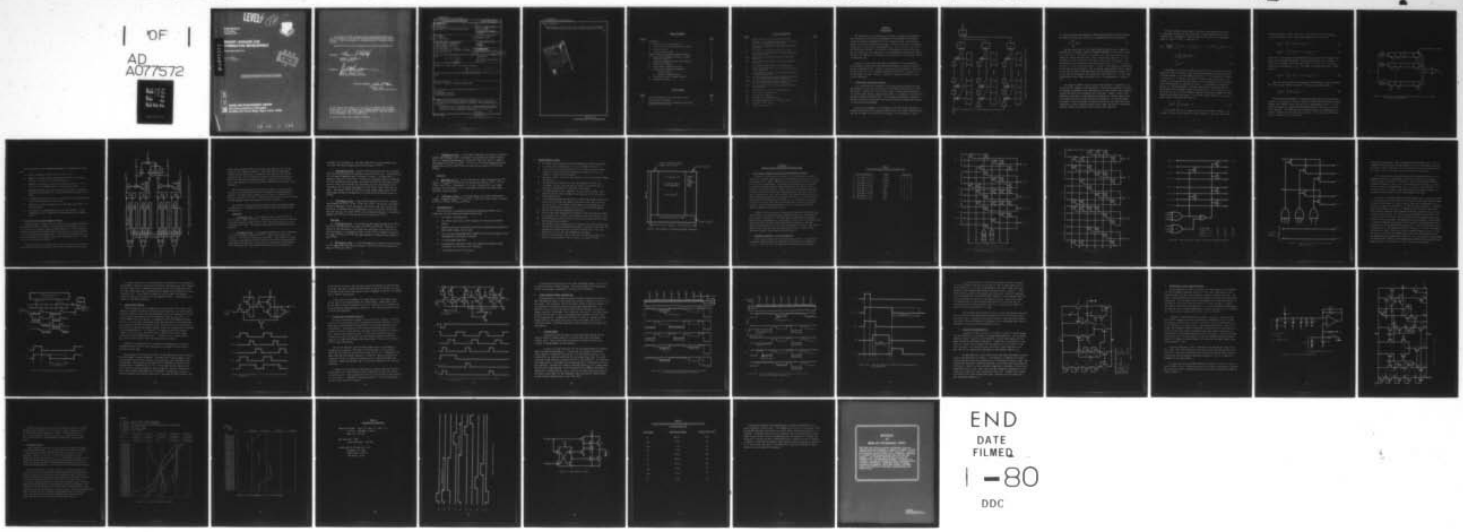

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RADC-TR-79-211
Interim Report
September 1979

BINARY/ANALOG CCD CORRELATOR DEVELOPMENT

Texas Instruments, Inc.

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: RADC-TR-79-211	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): BINARY/ANALOG CCD CORRELATOR DEVELOPMENT	5. TYPE OF REPORT & PERIOD COVERED: Interim Report 1 Aug 78 – 31 Jan 79
6. PERFORMING ORG. REPORT NUMBER: 08-79-10	
7. AUTHOR(s): R. A. Haken, R. C. Pettengill	8. CONTRACT OR GRANT NUMBER(s): F19628-78-C-0122
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Texas Instruments Incorporated, Central Research Laboratories, 13500 N. Central Expressway, Dallas TX 75265	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62702F, 46001826
11. CONTROLLING OFFICE NAME AND ADDRESS: Deputy for Electronic Technology (RADC/ESE), Hanscom AFB MA 01731	12. REPORT DATE: September 1979
	13. NUMBER OF PAGES: 49
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

TI-08-79-10

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Freeman Shepherd (ESE)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

CCD Filters
Programmable Correlators
Binary/Analog Correlator

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the design of a general-purpose, electronically programmable, 1024-bit binary/analog CCD correlator. The key features of the filter are:

Programmability of the reference signal, correlator length and weighting coefficient accuracy. This results in a filter with the flexibility to be operated in nine programmable configurations. → next page

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Item 20 (Continued)

Minimization of off-chip circuitry by including all analog and digital shift registers, clock drivers, logic, and output amplifiers on-chip.

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INTRODUCTION

The objectives of this program are to design, fabricate, and evaluate a general-purpose, electronically programmable, binary/analog CCD correlator. The device features programmability of the reference signal, the correlator length, and weighting coefficient accuracy. Off-chip circuitry is minimized by including all clock drivers, output-amplifiers, logic, and analog and digital shift registers, on-chip. This results in an integrated filter circuit that has the versatility to be operated in nine programmable configurations, thereby giving it the flexibility to be used in a wide variety of filtering and correlation applications.

Section I of this report describes the operation of the programmable binary/analog correlator and the architecture necessary to realize a general-purpose integrated filter. Section I concludes with a breakdown of the principal constituent cells of the general-purpose correlator and a summary of the accomplishments to date. Section II contains a technical discussion of the circuits designed.

A. Binary/Analog Correlator Operation

In a conventional CCD transversal filter the weighting coefficients are implemented by use of the well-known split electrode technique and are therefore fixed. Although such filters have a number of important applications in Air Force Systems, there are applications where it is necessary to electronically program the weighting coefficients. Of the present programmable techniques, the most attractive for matched filtering and correlation tracker applications is the binary/analog approach.

Electronic programmability is achieved in the binary/analog approach by decomposing each one of the weighting coefficients into a binary representation that can be loaded into a static shift register, as illustrated in Figure 1.

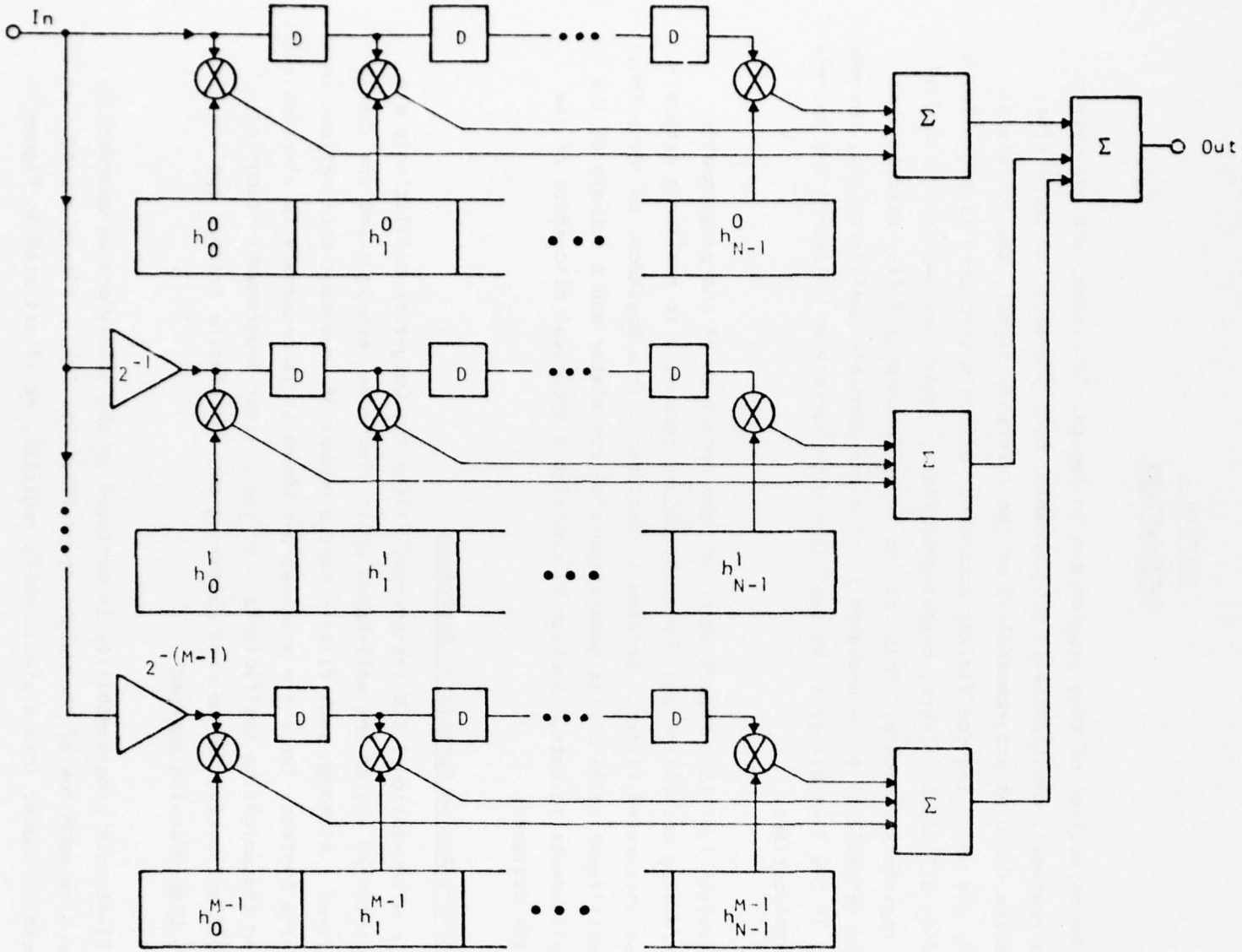


Figure 1 Block Diagram of the Binary/Analog Correlator

For M-bit accuracy of each weighting coefficient M parallel CCD binary/analog correlators are required, so that h_n is represented with M-bit accuracy by

$$h_n = \sum_{k=0}^{M-1} h_n^k \, 2^{-k} \quad . \tag{1}$$

The most significant bit h_n^0 of each weighting coefficient is loaded into the static shift register, shown as elongated rectangles in the filter at the top of the figure. The second most significant bit h_n^1 of each coefficient is loaded into the second coefficient store, and the least significant bit h_n^{M-1} is loaded into the coefficient store shown at the bottom of the figure. The analog signal must be weighted by the appropriate factor of $2^{-(n-1)}$ at either the input or output of each correlator. In Figure 1 the weighting is performed at the input to the correlators, with the analog signal applied without attenuation to the top filter (most significant bit) and attenuated by a factor of two at the input of the second filter (second most significant bit). At the input to the bottom filter (least significant bit) it is attenuated by a factor of 2^{M-1}.

The choice of whether input or output signal weighting is employed, or a mixture of both, depends on the application. Input signal weighting is simpler to implement as capacitor ratio techniques can be used, whereas output weighting requires amplifiers with accurately controlled gain. However, output signal weighting is desirable in some applications because of a dynamic range limitation associated with the input weighting configuration. For general-purpose correlators it may be desirable to perform a mixture of both input and output weighting to strike a balance between dynamic range, the number of integrators required, weighting coefficient accuracy, and logic simplicity.

The total weighting coefficient for any one of the M parallel CCD bits is determined by the sum of the coefficients in the M parallel static shift register bits. Consequently, when the outputs of each filter are summed together as shown in Figure 1, the result is

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \sum_{n=1}^{N} h_n^0 z^{-n} + 2^{-1} \sum_{n=1}^{N} h_n^1 z^{-n} + \ldots + 2^{-(M-1)} \sum_{n=1}^{N} h_n^{M-1} z^{-n} \quad (2)$$

$$= \sum_{n=1}^{N} \left[\sum_{k=0}^{M-1} \left(h_n^k 2^{-k} \right) \right] z^{-n} \quad (3)$$

$$= \sum_{n=1}^{N} h_n z^{-n} \quad . \quad (4)$$

Programmability of the CCD weighting coefficients is achieved by using the coefficient code in the static shift register to determine the relative timing of charge transfer in the four-phase CCD register. This is described in detail in Section II.B. In essence, the coefficient code in each of the static shift register cells determines when the charge in the corresponding CCD bit transfers to the electrode that is connected to the DCI. If the charge is transferred early at t_1, the charge packet is sampled underneath the sense electrode and contributes to the integrator output during that cycle. If the charge is transferred late at t_2, after the integrator sampling period has finished, the charge does not contribute to the output. In the time interval between t_1 and t_2 the output signal is available and given by:

$$Q_{out}(n) = \sum_{i=1}^{N} h_i Q_{sig}(n - i) \quad . \quad (5)$$

As described thus far, the device can only handle unipolar signals. For a signal of either sign to be used it must be added to a fat zero, which also

improves the charge transfer efficiency. The actual CCD input is then $Q_{sig} + Q_{FZ}$ and the output from a single binary/analog filter is given by:

$$Q_{out}(n) = \sum_{i=1}^{N} h_i \left[(Q_{FZ} + Q_{sig})(n - i) \right] \tag{6}$$

$$Q_{out}(n) = \sum_{i=1}^{N} h_i Q_{FZ} (n - i) + h_i Q_{sig} (n - i) \quad . \tag{7}$$

The first term represents a code-dependent offset and must be eliminated. The second term is the desired signal. To eliminate the first term, a parallel filter must be added in which the input signal is inverted, i.e., the input to the second CCD becomes $Q_{FZ} - Q_{sig}$. The output of the parallel filter is then given by:

$$Q_{out}(n) = \sum_{i=1}^{N} h_i Q_{FZ} (n - i) - h_i Q_{sig} (n - i) \quad . \tag{8}$$

When the two CCD outputs are connected to a differential current integrator, the undesired terms cancel, resulting in the DCI output being given by

$$Q_{out}(n) = \sum_{i=1}^{N} 2h_i Q_{sig} (n - i) \quad . \tag{9}$$

The differential approach for implementing coefficients with multiple-bit accuracy is illustrated in Figure 2, where the configuration correlates N analog samples with N digital words, each of which is represented by M-bits. In this scheme the weighting is applied to the analog signals at the input of the CCD shift registers. The summing of the M parallel channels is accomplished by a parallel connection of the ϕ_4^+ and ϕ_4^- clock buses. Thus, only one differential current integrator (DCI) is required.

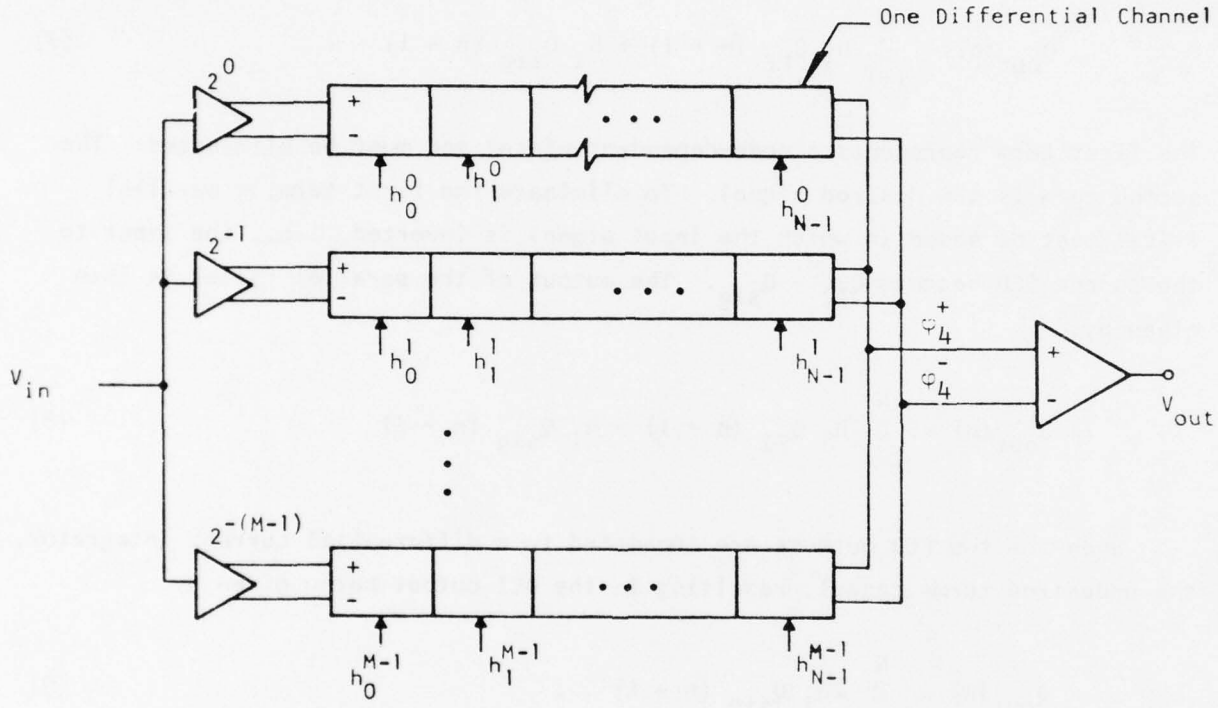


Figure 2 Schematic of a Programmable CCD Correlator with M-bit Accuracy on the Weighting Coefficients

The salient points of the binary/analog approach to programmable correlators are:

- One-bit programmable filters in which h_n can be 1 or 0.
- Capability to expand to M-bit accuracy by combining M binary/analog correlators in parallel with the appropriate gain.
- Capability to program the filters to the desired length (N = 32, 64, 128, etc.) and to cascade filters to achieve longer filters.
- Weighting coefficient accuracy sufficient to give eight-bit resolution on weighting coefficients (i.e., weighting coefficient accuracy of 0.2%, $\frac{1}{2}$ LSB).
- Minimization of off-chip circuitry. All clock drivers, output amplifiers, static shift registers, etc., are on-chip.
- Capability to utilize a microprocessor to read data out of memory into the code registers.
- Elimination of the code-dependent output dc level problem. A code-independent dc level is essential for spread spectrum and ECM applications.

B. Architecture for a General-Purpose Correlator

A general-purpose architecture for an electronically programmable 1024-stage binary/analog correlator is shown in the simplified block diagram of Figure 3. The architecture is arranged so that the 1024-stage device is folded into eight 128-stage sections with the output of each section fed via a unity gain amplifier to the input of the next 128-stage device. This provides a convenient point to insert an alternative input signal, together with the necessary logic for selecting the filter configuration desired.

To achieve multiple-bit accuracy, some of the signal weighting is performed at the input and some at the output, as this yields the optimum balance between

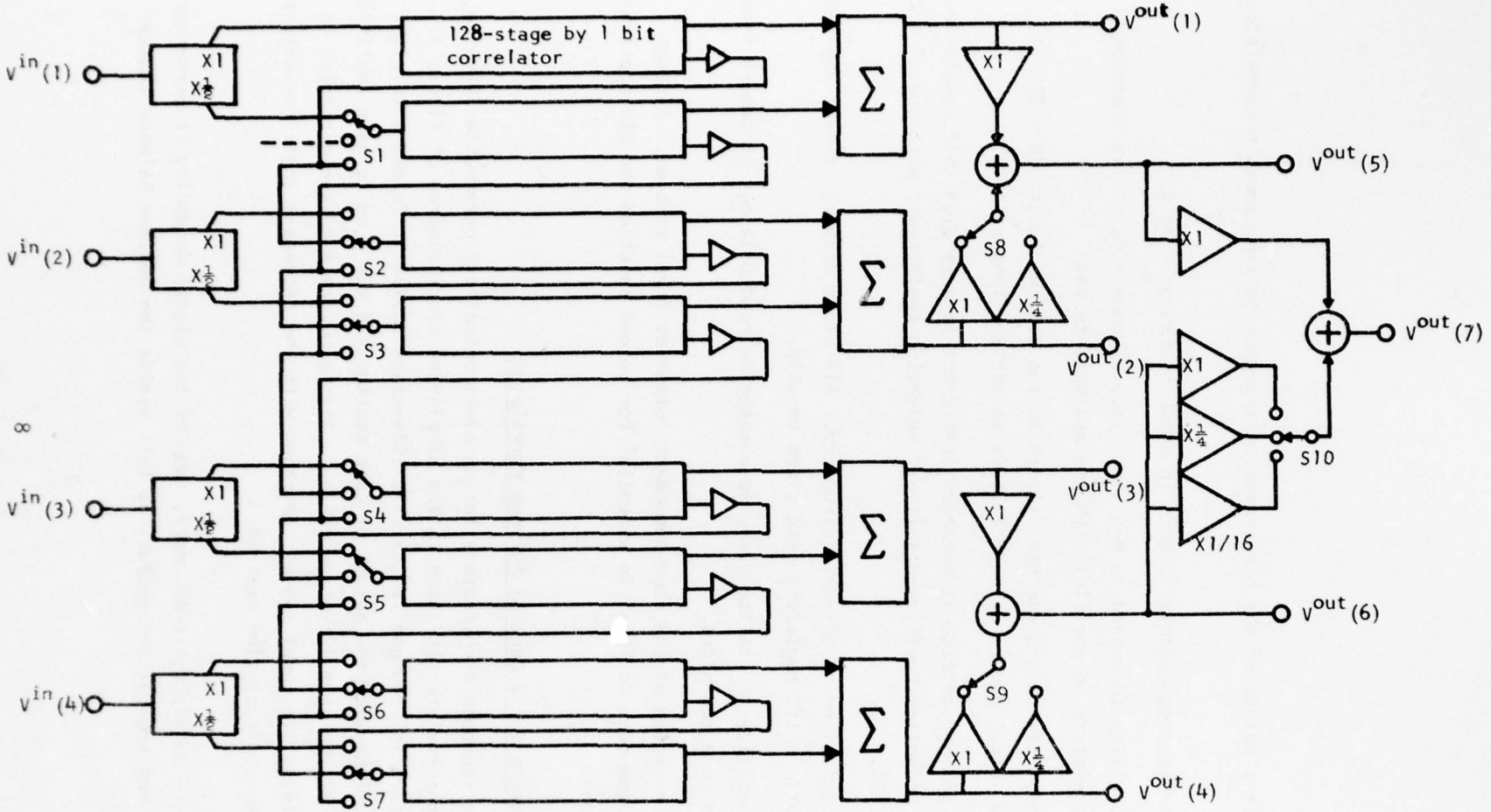


Figure 3 Analog Signal Flowgraph of 1024-Stage Binary/Analog Correlator (shown connected as a 256-stage by four-bit correlator)

dynamic range, weighting coefficient accuracy, the number of DCIs, and logic simplicity. The rectangles labeled X1, $X\frac{1}{2}$ through which the input passes indicate that the input signal is passed with unity gain (X1) and with 50% attenuation ($X\frac{1}{2}$). The input selection switches to the correlators determine whether the attenuated or unattenuated signal is applied to the correlator input. The remainder of the signal weighting is performed at the output of the correlators.

The correlation outputs of the correlators (output at the top of each correlator) go to the differential current integrators and summing amplifiers labeled Σ. By summing the correlation outputs in pairs, the number of DCI amplifiers required is only four. The DCI outputs are summed through two switched, weighted summation stages that determine the mode of operation.

The flexibility of the architecture chosen to realize the general-purpose correlator chip is illustrated by the nine possible operating configurations described below.

Single Mode

1. 1024-stage by 1 bit. In this mode the input is applied to $V^{in}(1)$, and the output is taken from $V^{out}(7)$. The inputs to each correlator are switched to the lower position so that the serial output from the preceding correlator is applied to the input. The switches on the outputs all select the unity gain amplifiers.

2. 512-stage by 2 bits. In this mode of operation the input is applied to $V^{in}(1)$, and the output is taken from $V^{out}(7)$. The X1 input is applied to correlator 1, and $X\frac{1}{2}$ input is applied to correlator 2. The inputs of all other correlators are switched to the central position such that the unattenuated (X1) signal passes from correlator 1 to correlator 3 to correlator 5 to correlator 7, and the attenuated ($X\frac{1}{2}$) signal passes from correlator 2 to correlator 4 to

correlator 6 to correlator 8. The output amplifiers are all switched to the unity gain setting and summed to provide the output at $V^{out}(7)$.

3. 256-stage by 4 bits. Four-bit and 8-bit operation are the only modes that utilize output amplifier settings at other than unity gain. The connections for this mode of operation are illustrated in Figure 3. The same input is applied to both $V^{in}(1)$ and $V^{in}(3)$. The top four correlators perform a 256-stage by 2-bit correlation with the most significant bit (MSB) and the second significant bit (2SB), and the bottom four correlators perform a 256-stage by 2-bit correlation with the third significant bit (3SB) and the least significant bit (LSB). The outputs $V^{out}(5)$ and $V^{out}(6)$ are then summed together with $V^{out}(6)$ being summed through the $X\frac{1}{4}$ amplifier to provide the 4-bit weighted output at $V^{out}(7)$.

4. 128-stage by 8 bits. In this mode of operation the input is applied simultaneously to $V^{in}(1)$, $V^{in}(2)$, $V^{in}(3)$, and $V^{in}(4)$. The top four correlators perform a 128-stage by 4-bit correlation with the MSB, 2SB, 3SB, and 4SB; the bottom four correlators perform a 128-stage by 4-bit correlation with the 5SB, 6SB, 7SB, and LSB. The output $V^{out}(6)$ is then summed through the X1/16 amplifier, together with $V^{out}(5)$, to provide the 8-bit correlation at $V^{out}(7)$.

Dual Mode

5. 512-stage by 1 bit. In this mode the two inputs are applied to $V^{in}(1)$ and $V^{in}(3)$, and the outputs are taken from $V^{out}(5)$ and $V^{out}(6)$. Operation is similar to the 1024-stage by 1 bit except that the switch at the input to the fifth correlator is in the upper position so that $V^{in}(3)$ is applied to the input. The outputs $V^{out}(5)$ and $V^{out}(6)$ are taken separately instead of being summed to give $V^{out}(7)$.

6. 256-stage by 2 bits. In this mode operation is similar to the 512-stage by 2-bit mode except that inputs are made at $V^{in}(1)$ and $V^{in}(3)$, and outputs are taken at $V^{out}(5)$ and $V^{out}(6)$.

7. 128-stage by 4 bits. In this mode of operation the top four correlators perform one 128-stage by 4-bit correlation and the bottom four perform another. Input 1 is applied simultaneously to $V^{in}(1)$ and $V^{in}(2)$, and input 2 is applied simultaneously to $V^{in}(3)$ and $V^{in}(4)$. $V^{out}(2)$ and $V^{out}(4)$ are summed through the $X\frac{1}{4}$ amplifier to $V^{out}(1)$ and $V^{out}(3)$ to provide the two outputs at $V^{out}(5)$ and $V^{out}(6)$.

Quad Mode

8. 256-stage by 1 bit. In this mode the four inputs are applied to $V^{in}(1)$, $V^{in}(2)$, $V^{in}(3)$, and $V^{in}(4)$; and the four outputs are taken at $V^{out}(1)$, $V^{out}(2)$, $V^{out}(3)$, and $V^{out}(4)$. Correlators 1, 3, 5, and 7 select the X1 input (upper position); and correlators 2, 4, 6, and 8 select the output from the previous correlator (lower position).

9. 128-stage by 2 bits. In this mode the pairs of filters operate separately. Inputs are made at $V^{in}(1)$, $V^{in}(2)$, $V^{in}(3)$, and $V^{in}(4)$; outputs are taken at $V^{out}(1)$, $V^{out}(2)$, $V^{out}(3)$, and $V^{out}(4)$.

C. Constituent Cells

The architecture of the general-purpose binary/analog correlator can be broken down into the following principal on-chip cells.

- 16 x 128-bit four-phase CCDs
- 16 x 64-bit static binary shift registers for storing the reference signal
- Switching circuitry for selecting the filter configuration and operating mode; either single, dual or quad
- 16 x unity gain charge amplifiers (CVAMPs) for linking the output of one 128-stage CCD to the input of the next
- 7 x DCIs/summing amplifiers
- Microprocessor interface circuitry for loading the reference signal from memory into the static shift registers
- Clock generation and drive circuits.

D. Accomplishments to Date

- An overall layout scheme has been developed (see Figure 4) resulting in a chip size of approximately 7.1 x 6.2 mm^2 (280 x 245 $mils^2$).
- A bus line structure has been devised that strikes a balance between length of routing (and hence resistance and capacitance) with the number of crossovers and crossunders.
- The input, output, and filter mode selection circuitry has been designed and laid out.
- The digital shift-register cell has been designed, laid out, and simulated. The cell has also been included on a TI-funded test bar and should be available for evaluation during March.
- The CVAMP design has been completed, laid out, and simulated. This amplifier has also been included on the same test bar as the digital shift-register cell.
- A clocking scheme has been devised for shifting the charge from the output of one CCD through the CVAMP to the input of the next CCD during one clock cycle. This scheme allows charge to move through only one CCD bit and therefore prevents the loss of any correlation samples.
- The CCD cells have been designed and laid out.
- Circuitry has been designed and simulated to allow the reference signal to be loaded into the static shift-register under microprocessor control.
- The differential current integrators and output-summing amplifiers have been designed and simulated.
- The complete clocking requirements of the device have been evaluated and the various loading capacitances calculated. The clock drivers have been designed and simulated and are currently being laid out. The clock generation circuitry has been designed and simulated.
- Accuracy considerations require that the X1 and $X\frac{1}{2}$ signal amplifiers, which are located ahead of the correlators, be placed off-chip.

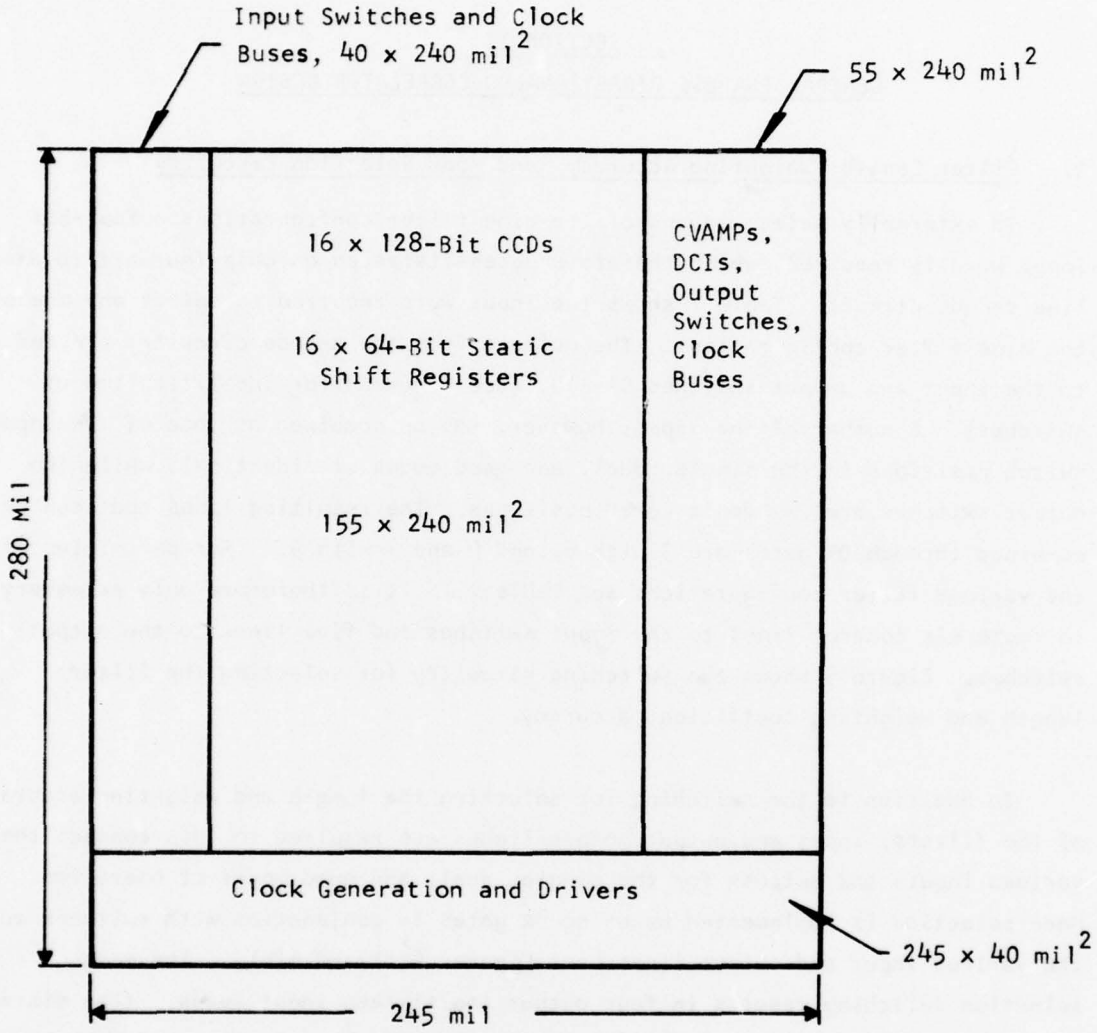


Figure 4 Chip Layout of the General-Purpose Correlator

SECTION II

GENERAL PURPOSE BINARY/ANALOG CORRELATOR DESIGN

A. Filter Length, Weighting Accuracy, and Mode Selection Circuitry

To externally select anyone of the nine filter configurations a four-bit input word is required, which therefore necessitates an on-chip four-bit to nine-line decode circuit. Table 1 shows the input word required to select any one of the nine filter configurations. The outputs from the decode circuitry are fed to the input and output switches S1-S10, (see Figure 3 for identification of switches). A number of the lines, however, may be combined as some of the input switch positions in the single, dual, and quad modes are identical, while the output switches are in "don't care" positions. The resulting lines that can be combined through OR gates are 3 with 6, and 4 and 7 with 9. (For definition of the various filter configurations see Table 1.) It is therefore only necessary to route six control lines to the input switches and five lines to the output switches. Figure 5 shows the switching circuitry for selecting the filter length and weighting coefficient accuracy.

In addition to the switching for selecting the length and weighting accuracy of the filters, input and output mode switches are required to interconnect the various inputs and outputs for the single, dual, and quad modes of operation. Mode selection is implemented by using OR gates in conjunction with switches across the various input and output lines [see Figures 6(a) and 6(b)]. The mode selection switching results in four output and sixteen input leads. (The sixteen inputs are due to the X1 and $X\frac{1}{2}$ functions being off-chip; in Figure 3 each 128-stage correlator incorporates a differential pair.)

B. Programmable Weighting Using a Four-Phase CCD

In the original proposal for the binary/analog correlator, No. 23-R77, the programmable weighting scheme was discussed with reference to a two-phase CCD structure. Since that time a four-phase CCD technology has been developed,

Table 1

Filter Configuration Versus Input Select Word

Filter Configuration	Mode	Input Word A	B	C	D
(1) 1024-stage by 1-bit	Single	1	0	0	0
(2) 512-stage by 2 bits	Single	0	1	0	0
(3) 256-stage by 4 bits	Single	1	1	0	0
(4) 128-stage by 8 bits	Single	0	0	1	0
(5) 512-stage by 1 bit	Dual	1	0	1	0
(6) 256-stage by 2 bits	Dual	0	1	1	0
(7) 128-stage by 4 bits	Dual	1	1	1	0
(8) 256-stage by 1 bit	Quad	0	0	0	1
(9) 128-stage by 2 bits	Quad	1	0	0	1

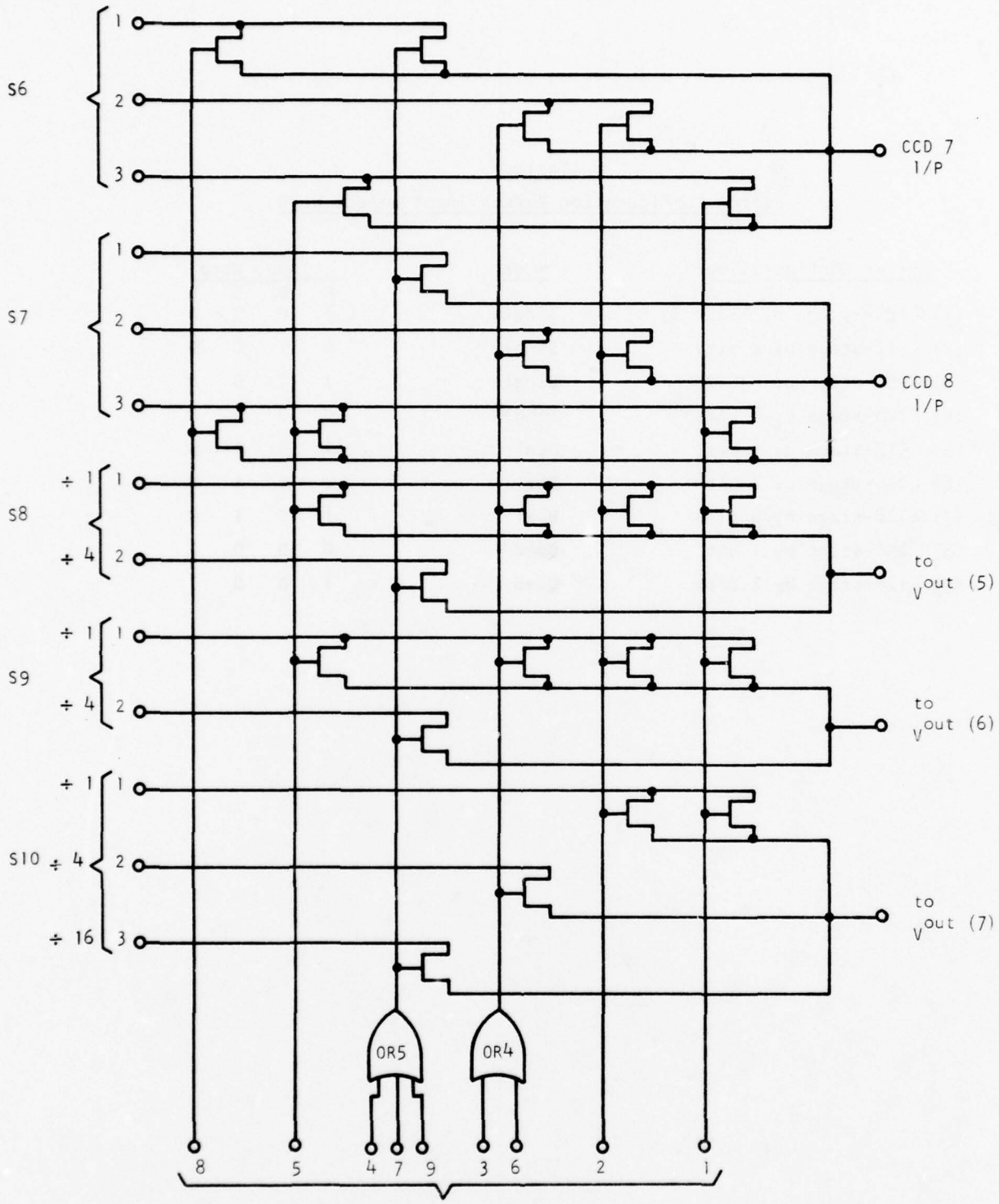
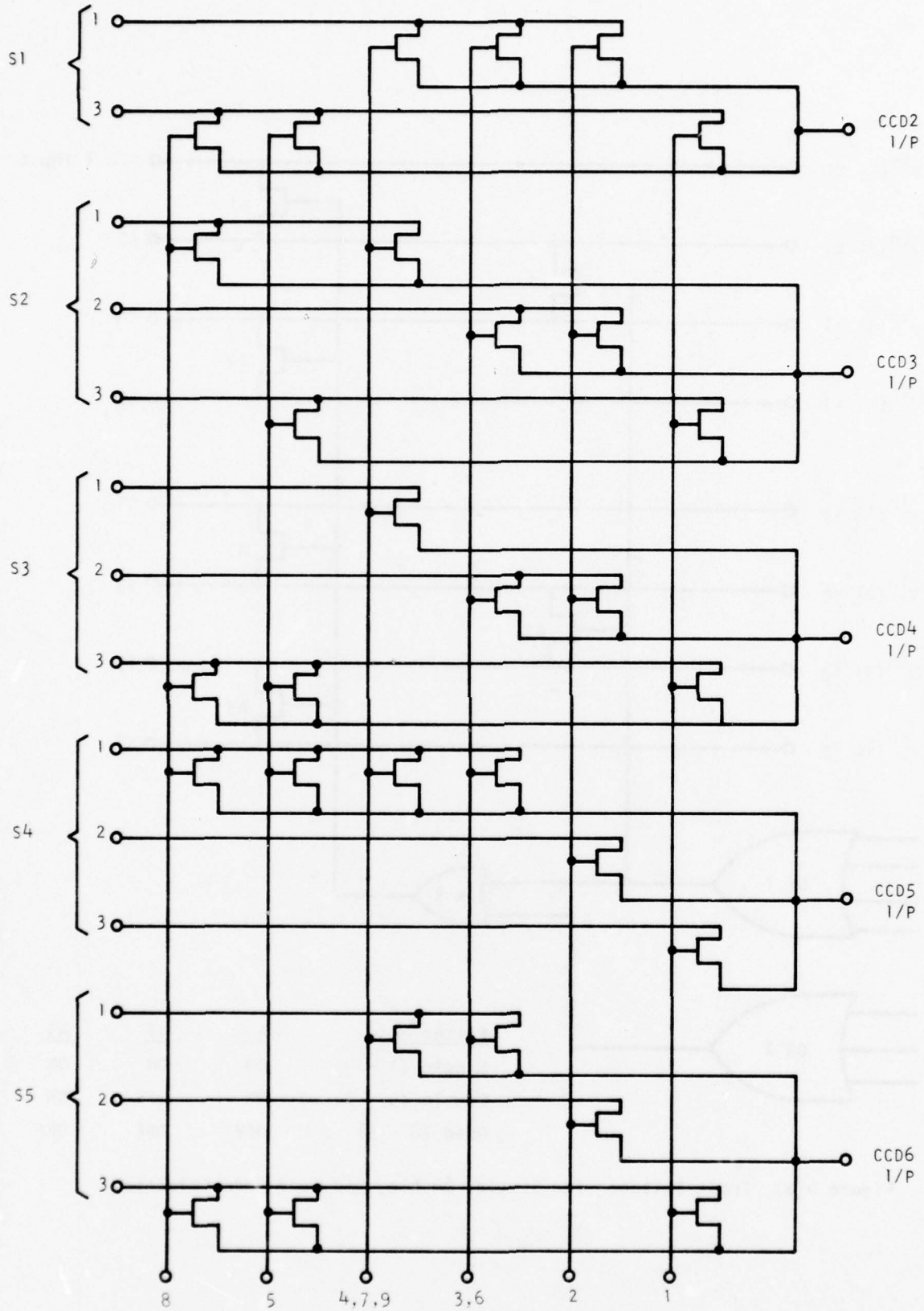


Figure 5 Circuitry for Selecting Filter Length and Weighting Coefficient Accuracy



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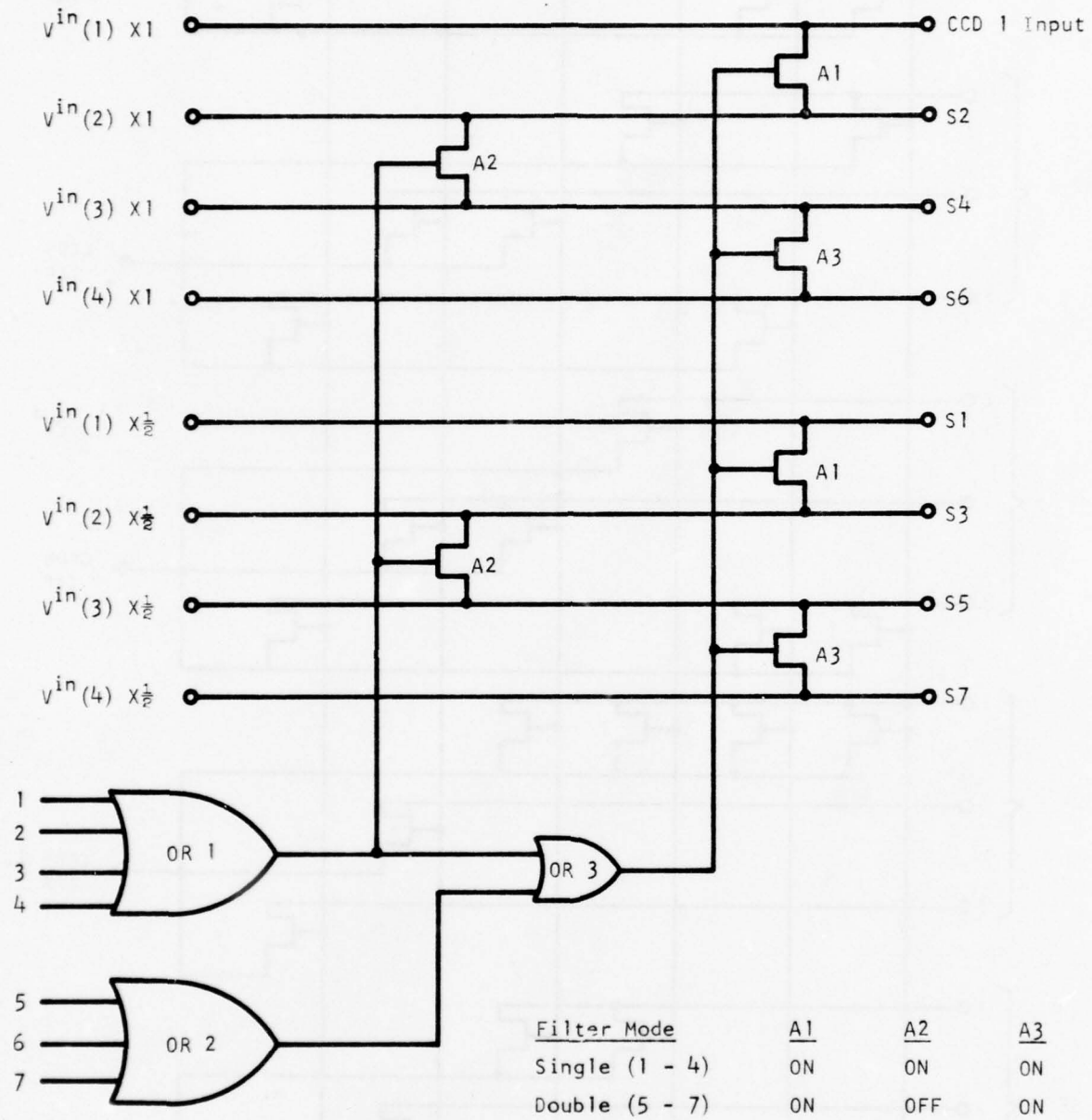


Filter Mode	A1	A2	A3
Single (1 - 4)	ON	ON	ON
Double (5 - 7)	ON	OFF	ON
Quad (8 - 9)	OFF	OFF	OFF

Figure 6(a) Input Switches for Single, Double, and Quad Mode Selection

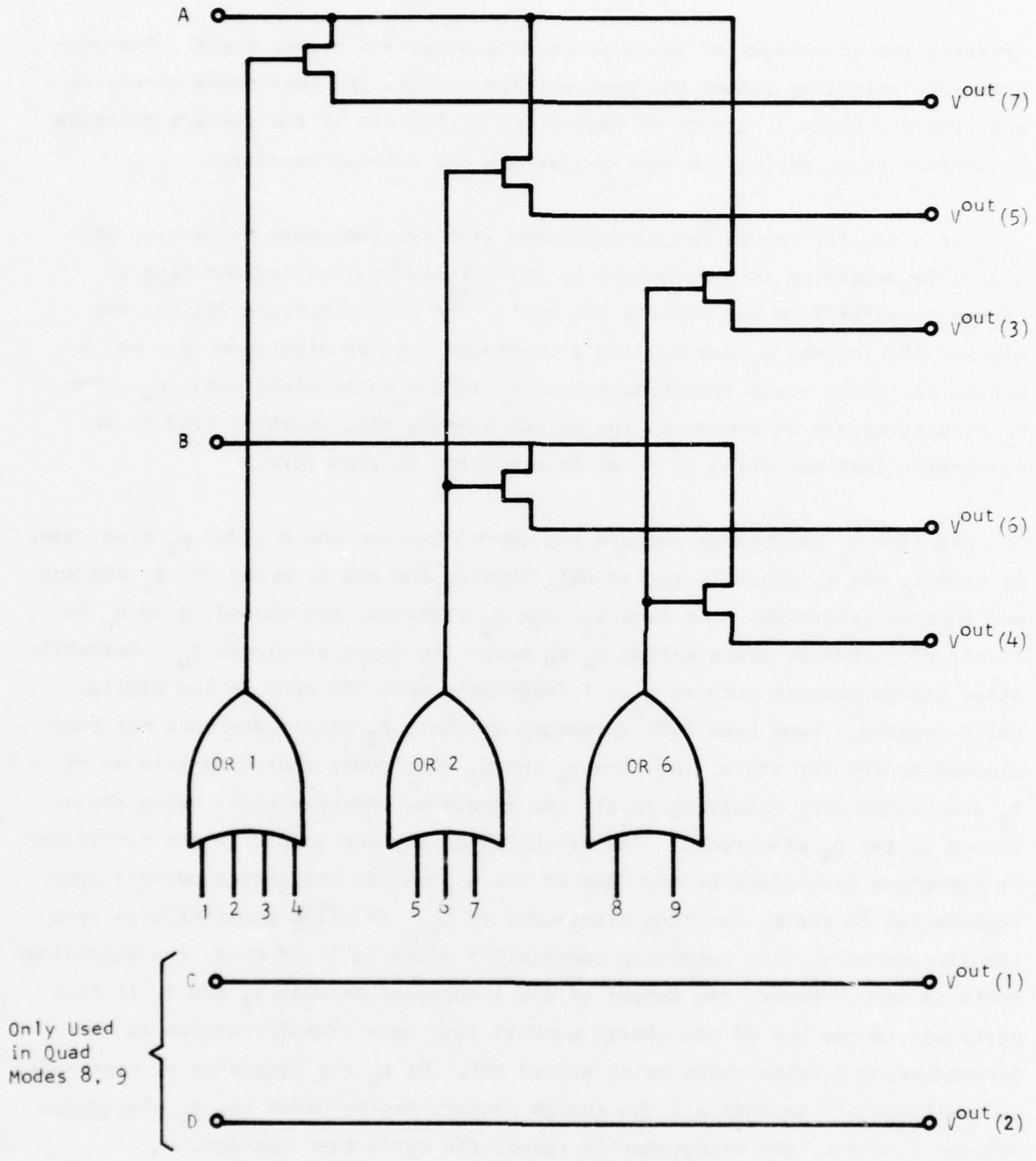


Figure 6(b) Output Switches for Single, Double, and Quad Mode Selection

offering the advantages of fewer processing steps and higher yield. The programmable weighting scheme has been adapted to suit the four-phase structure, and Figure 7 shows a section of such a CCD with plots of the surface potential at various times during charge transfer and the driving waveforms.

In a similar way as was accomplished with the two-phase structure, programmable weighting is implemented by selectively controlling the time of charge transfer from one well to the next. The four-electrode CCD has two clocked electrodes, ϕ_1 and ϕ_2, and a dc-biased barrier electrode, ϕ_3, which serves to reduce clock feedthrough from ϕ_2 to the sense electrodes, ϕ_4. The ϕ_4 electrodes are in common on the output summing bus, which is tied to an integrator that maintains it at an intermediate dc bias level.

At time t_1 the charge packets are shared between the ϕ_1, and ϕ_2 electrodes. At time t_2 the ϕ_1 clock is turned off, leaving the charge under the ϕ_2 storage and control electrodes. At time t_3, the ϕ_2 electrode corresponding to q_n is turned off, thereby transferring q_n to under the sense electrode ϕ_4. Meanwhile, other charge packets such as $q_n + 1$ (depending upon the code in the digital shift-register) have been left unchanged as those ϕ_2 electrodes have not been clocked to the off state. At time t_4 the ϕ_2 electrodes that were held on at t_3 are turned off, resulting in all the remaining charge packets being transferred to the ϕ_4 electrodes. The weighting on any one sample in the correlator is therefore determined by how many of the M parallel CCD charge packets were transferred to the ϕ_4 sampling electrodes at t_3. If all M parallel bits were transferred at t_3, the weighting coefficient would be 1; if none, the weighting would be zero. Hence, the output of the integrator between t_3 and t_4 is proportional to the sum of the charge packets that were transferred due to the corresponding ϕ_2 electrodes being turned off. At t_4 the remaining ϕ_2 electrodes are switched off so that all the charge packets reside under the ϕ_4 electrodes. Between t_4 and t_1 the integrator is reset; the cycle then repeats.

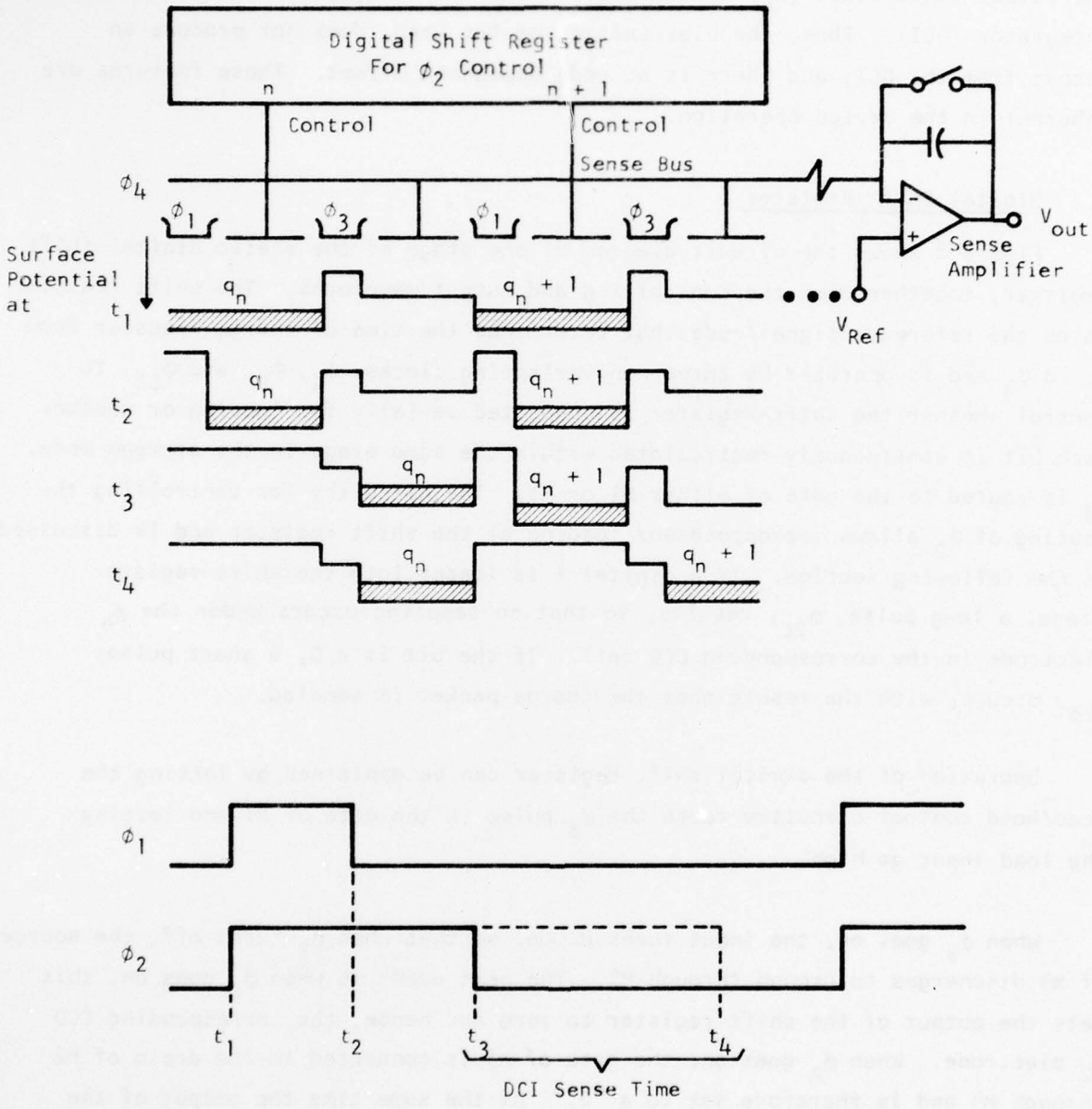


Figure 7 Programmable Weighting Using a Four-Phase CCD

As noted in Section I.A, for each section of the correlator two CCD channels are operated in parallel, both being controlled by the same digital shift-register. The input signal and its complement are applied to the two CCD channels, while the output sense buses (ϕ_4) are differentially summed by the differential current integrator (DCI). Thus, the bias charge, or fat zero, does not produce an output from the DCI; and there is no code dependent offset. These features are inherent in the device operation.

C. Digital Shift Register

Figure 8 shows the circuit diagram of one stage of the static digital shift register, together with the controlling and output waveforms. The shift register holds the reference signal/code that determines the time of charge transfer from ϕ_2 to ϕ_4 and is operated by three nonoverlapping clocks, ϕ_A, ϕ_B, and ϕ_C. To control whether the shift-register is connected serially for loading or whether each bit is continuously recirculated within the same stage in the storage mode, ϕ_B is routed to the gate of either M1 or M8. The circuitry for controlling the routing of ϕ_B allows microprocessor loading of the shift register and is discussed in the following section. If a digital 1 is loaded into the shift register stage, a long pulse, ϕ_{2L}, results, so that no sampling occurs under the ϕ_4 electrode in the corresponding CCD cell. If the bit is a 0, a short pulse, ϕ_{2S}, occurs, with the result that the charge packet is sampled.

Operation of the digital shift register can be explained by letting the load/hold control circuitry route the ϕ_B pulse to the gate of M1 and letting the load input go high.

When ϕ_B goes on, the input turns M2 on, so that when ϕ_B turns off, the source of M3 discharges to ground through M2. The next event is when ϕ_C goes on, this sets the output of the shift register to zero and hence, the corresponding CCD ϕ_2 electrode. When ϕ_A goes on, the gate of M5 is connected to the drain of M2 through M4 and is therefore set to a "0." At the same time the output of the shift register tracks ϕ_A through M6. When ϕ_A goes off, the shift register output is left floating high because M5 is turned off. Consequently, a long ϕ_2 pulse is generated; only when ϕ_C comes on will the output be reset to zero. Now

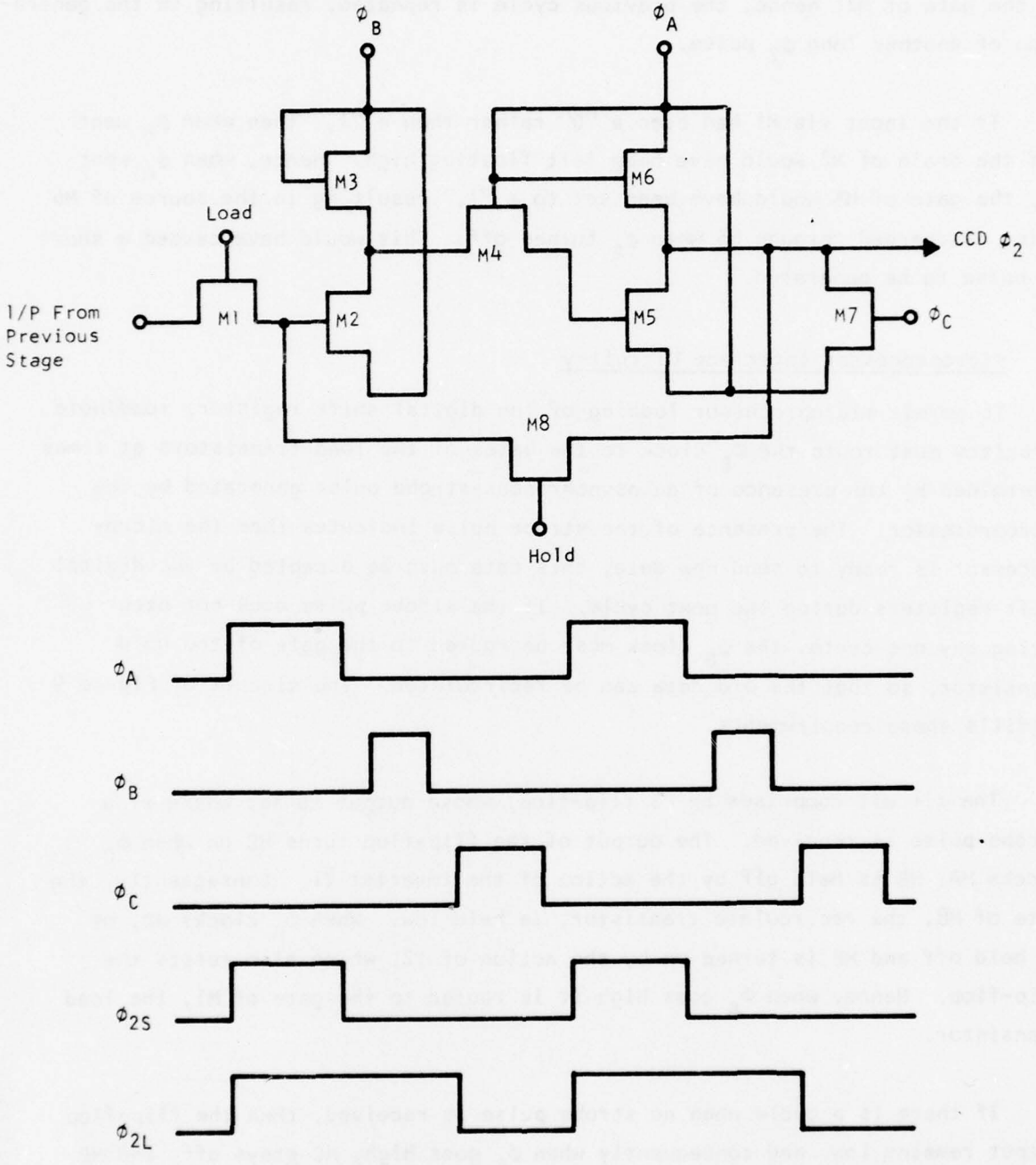


Figure 8 Digital Shift Register Circuit with Controlling and Output Waveforms

let the control circuitry route the next ϕ_B pulse to the gate of the hold transistor M8. When M8 is clocked, the high output of the shift register is routed to the gate of M2; hence, the previous cycle is repeated, resulting in the generation of another long ϕ_2 pulse.

If the input via M1 had been a "0" rather than a "1," then when ϕ_B went off the drain of M2 would have been left floating high. Hence, when ϕ_A went on, the gate of M5 would have been set to a "1," resulting in the source of M6 being discharged through M5 when ϕ_A turned off. This would have caused a short ϕ_2 pulse to be generated.

D. Microprocessor Interface Circuitry

To permit microprocessor loading of the digital shift register, load/hold circuitry must route the ϕ_B clock to the gates of the load transistors at times determined by the presence of an asynchronous strobe pulse generated by the microprocessor. The presence of the strobe pulse indicates that the microprocessor is ready to send new data; this data must be accepted by the digital shift registers during the next cycle. If the strobe pulse does not occur during any one cycle, the ϕ_B clock must be routed to the gate of the hold transistor, so that the old data can be recirculated. The circuit of Figure 9 fulfills these requirements.

The circuit comprises an RS flip-flop, whose output is set whenever a strobe pulse is received. The output of the flip-flop turns MC on when ϕ_C clocks MA; MB is held off by the action of the inverter I1. Consequently, the gate of M8, the recirculate transistor, is held low. When ϕ_A clocks MD, MF is held off and ME is turned on by the action of I2, which also resets the flip-flop. Hence, when ϕ_B goes high it is routed to the gate of M1, the load transistor.

If there is a cycle when no strobe pulse is received, then the flip-flop output remains low, and consequently when ϕ_C goes high, MC stays off, and MB is turned on by I1. When ϕ_A goes high, MF is turned on and ME, by the action of I2, is turned off. Consequently when ϕ_B goes high, it is routed through MB to the gate of M8, the hold transistor.

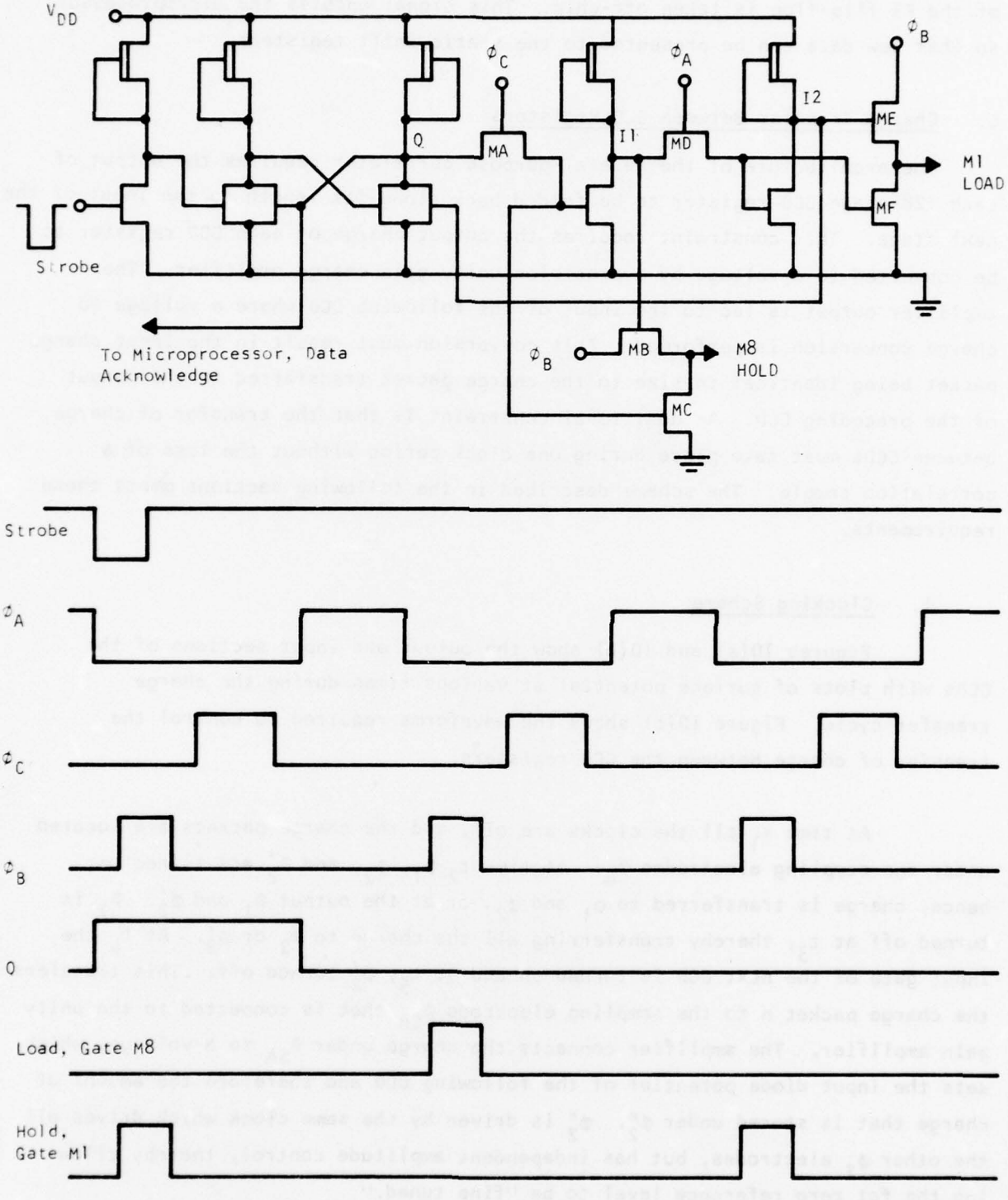


Figure 9 Microprocessor Interface Circuitry Showing Generation of Load and Hold Pulses

To provide the microprocessor with a data acknowledge signal, the Q output of the RS flip-flop is taken off-chip. This signal enables the microprocessor, so that new data can be presented to the static shift registers.

E. Charge Transfer Between CCD Registers

The architecture of the general-purpose correlator requires the output of each 128-stage CCD register to be folded back along its length to the input of the next stage. This constraint requires the output charge of each CCD register to be converted to a voltage by a precision unity gain charge amplifier. The amplifier output is fed to the input of the following CCD where a voltage to charge conversion is performed. This conversion must result in the input charge packet being identical in size to the charge packet transferred to the output of the preceding CCD. An additional constraint is that the transfer of charge between CCDs must take place during one clock period without the loss of a correlation sample. The scheme described in the following sections meets these requirements.

1. Clocking Scheme

Figures 10(a) and 10(b) show the output and input sections of the CCDs with plots of surface potential at various times during the charge transfer cycle. Figure 10(c) shows the waveforms required to control the transfer of charge between the CCD registers.

At time t_1 all the clocks are off, and the charge packets are located under the sampling electrodes ϕ_4. At time t_2 ϕ_1, ϕ_2, and ϕ_2' are turned on; hence, charge is transferred to ϕ_1 and ϕ_2, or at the output ϕ_1 and ϕ_2'. ϕ_1 is turned off at t_3, thereby transferring all the charge to ϕ_2 or ϕ_2'. At t_4 the input gate of the next CCD is turned on and at t_5, ϕ_2' turned off. This transfers the charge packet n to the sampling electrode ϕ_{SA} that is connected to the unity gain amplifier. The amplifier connects the charge under ϕ_{SA} to a voltage, which sets the input diode potential of the following CCD and therefore the amount of charge that is stored under ϕ_2''. ϕ_2'' is driven by the same clock which drives all the other ϕ_2 electrodes, but has independent amplitude control, thereby allowing the fat zero reference level to be "fine tuned."

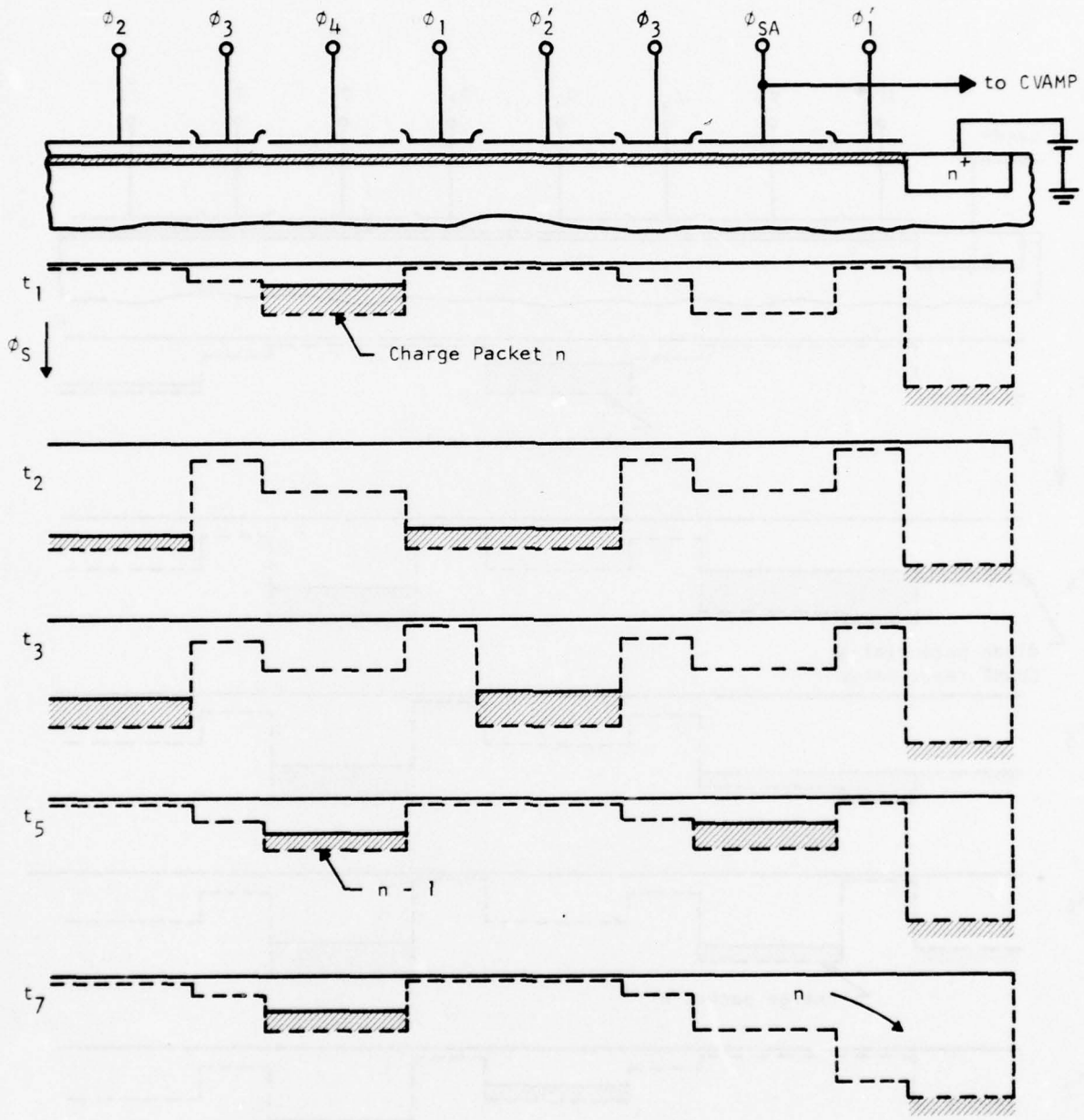


Figure 10(a) CCD Output Stage Showing Surface Potential Variations During Charge Transfer Between CCD Registers

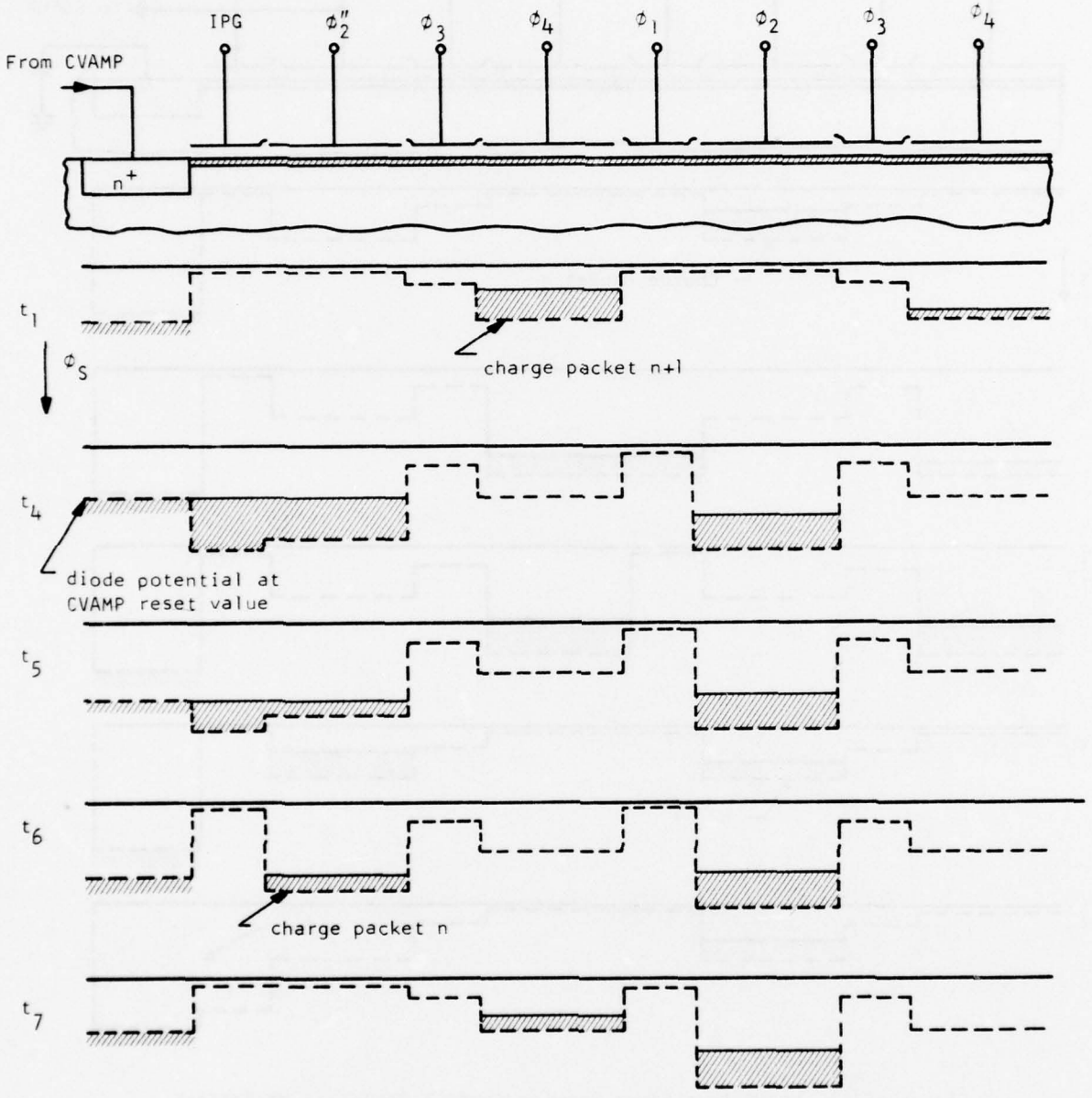


Figure 10(b) CCD Input Stage Showing Surface Potential Variations During Charge Transfer Between CCD Registers

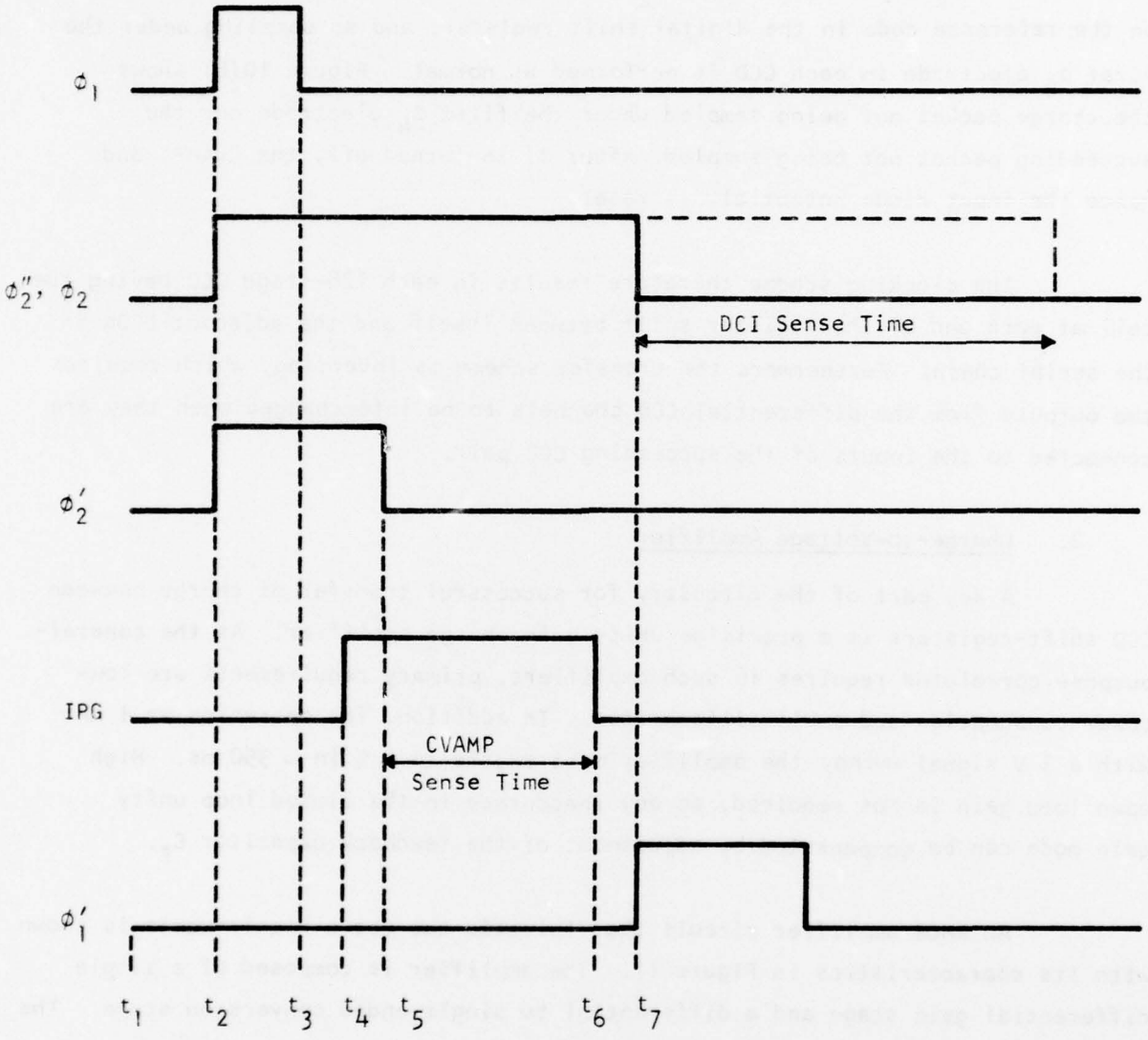


Figure 10(c) Clocking Scheme for Transferring Charge Between CCD Shift Registers

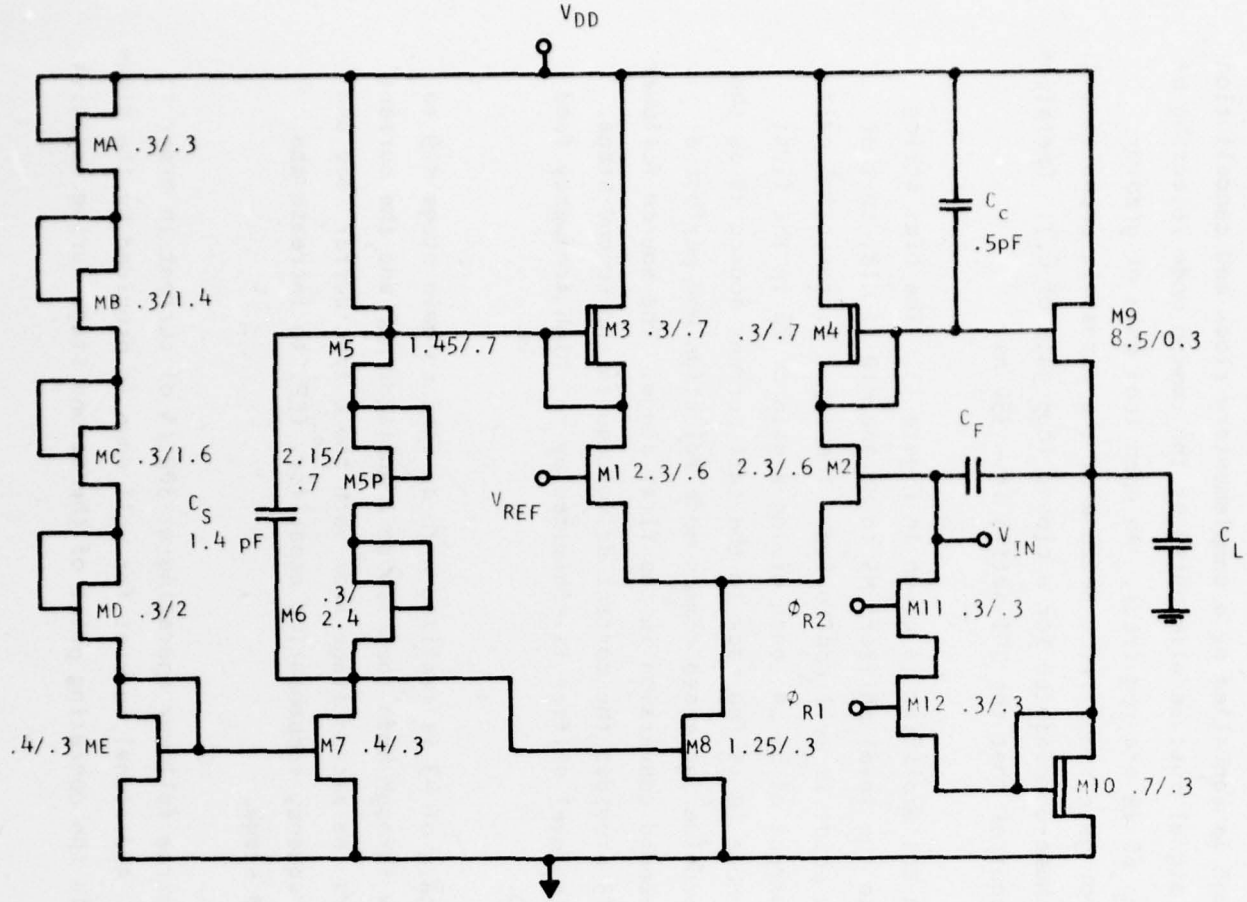
At t_6 the input gate is turned off and hence the CVAMP has between t_5 and t_6 to settle, which at a clock rate of 1 MHz is approximately 370 ns. ϕ_1' is turned on at t_7 so that the charge packet that was located under ϕ_{SA} is dumped into the reverse-biased diode at the end of the CCD register. At the same time the ϕ_2 clocks, including ϕ_2'', are selectively turned off, depending on the reference code in the digital shift register, and so sampling under the first ϕ_4 electrode in each CCD is performed as normal. Figure 10(b) shows the charge packet not being sampled under the first ϕ_4 electrode and the succeeding packet not being sampled. After ϕ_1' is turned off, the CVAMP, and hence the input diode potential, is reset.

The clocking scheme therefore results in each 128-stage CCD having the cell at each end of the register split between itself and the adjacent CCDs in the serial chain. Furthermore the transfer scheme is inverting, which requires the outputs from the differential CCD channels to be interchanged when they are connected to the inputs of the succeeding CCD pair.

2. Charge-to-Voltage Amplifier

A key part of the circuitry for successful transfer of charge between CCD shift-registers is a precision unity gain charge amplifier. As the general-purpose correlator requires 16 such amplifiers, primary requirements are low-power consumption and small-silicon area. In addition, for operation at 1 MHz with a 3 V signal swing, the amplifier must settle to 1 % in $\sim$ 350 ns. High open loop gain is not required, as any inaccuracy in the closed loop unity gain mode can be compensated by adjustment of the feedback capacitor C_F.

An NMOS amplifier circuit that fulfills the above requirements is shown with its characteristics in Figure 11. The amplifier is composed of a single differential gain stage and a differential to single-ended conversion stage. The feedback path between M1 and M8 also provides for improved common mode rejection. The output is taken via a source-follower stage that is designed to drive a load capacitance of up to 5 pF. Open loop unity gain frequency compensation is provided by C_c, which also limits the amplifier slew rate. The amplifier occupies an area of 0.5 mm^2 that includes both reset transistors and the closed loop gain adjustment capacitor C_F.



Charge Amplifier Characteristics

Power	6 mW
Open Loop Gain	40
Unity Gain Bandwidth	11 MHz
Slew Rate	20 v/μs
Phase Margin	50°
Load	5 pF
Silicon Area	0.05 mm^2

Figure 11 Charge Amplifier Circuit and Characteristics

F. Differential Current Integrator Design

The DCI amplifier is shown in Figure 12 with the related circuit elements. The 10.7 pF feedback capacitor allows a full 8 V output swing when a filter processing gain of 0.25 is used and maximum signal is present in the CCD. The Phase 1 clock feedthrough is cancelled by a complementary clock and cancellation capacitance. Fat zero signal must be eliminated by the common mode rejection of the amplifier (more than 60 dB are required). An open loop gain of greater than 1000 is required for gain stability. Because of the parasitic capacitances, the amplifier must be phase-compensated for a closed loop gain of 6.7. Operation at a 1 MHz data rate requires that the DCI settle in ~ 350 ns.

A schematic of the DCI amplifier is given in Figure 13. The bias string M14 to M18 is matched to the level shifters M5 to M8 and M10 to M13, so that the quiescent operating point is well controlled. The input differential pair M1 - M2 operate at a current of 65 μA, each giving a gain of 26 in the first stage. The voltage at node 10 is fed back to the tail current source M9 by the source follower M5 to provide increased common mode rejection and perform a differential to single-ended conversion in the first stage. The source follower level shifter M10 to M13 provides the correct dc voltage to the second stage. Phase shift through this level shifter is minimized by the high frequency feed forward capacitor, CLSO.

The second stage gain of 43 is realized with an enhance gain stage M19 to M22. About 130 μA flow through both the cascode transistor M20 and the current source M21. M27 buffers the second stage from both the output buffer load and a portion of the low frequency compensating capacitor, CCF, to increase the bandwidth of the second stage.

The output is a source follower operating at 300 μA of current in order to drive a load of 15 pF. Additional current for pull down is provided by the diode MLS, which also controls the operating point of the second stage during negative output slewing.

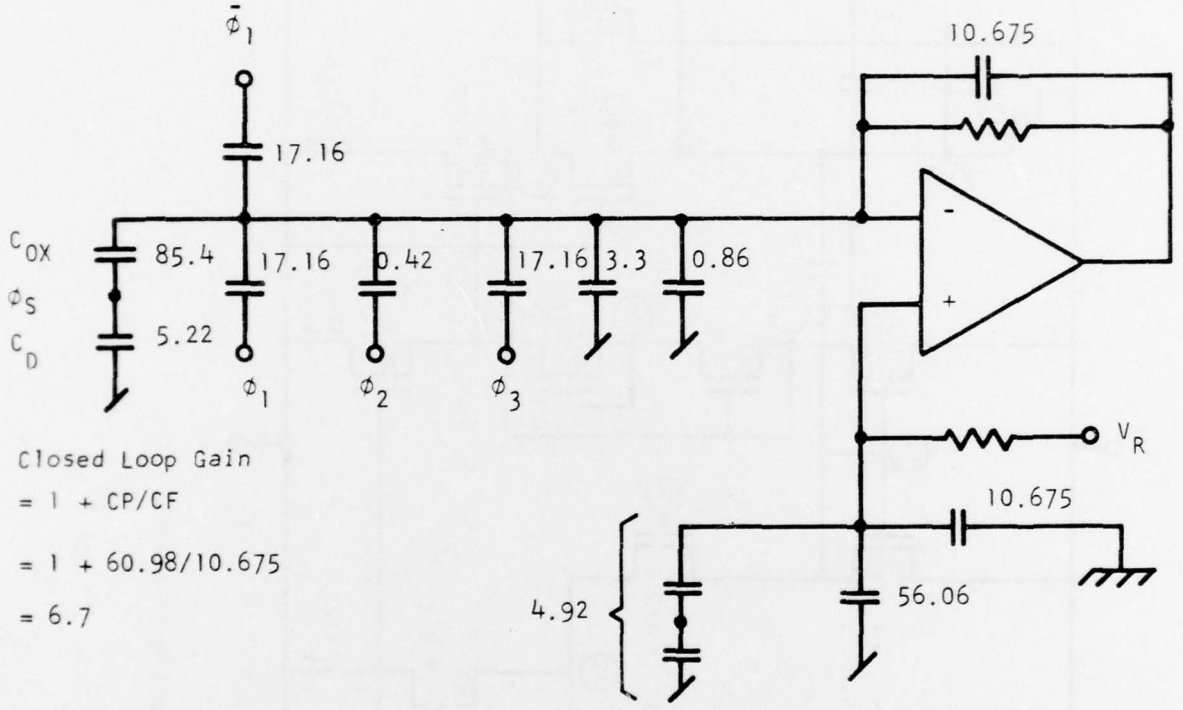


Figure 12 DCI Circuit with Parasitics

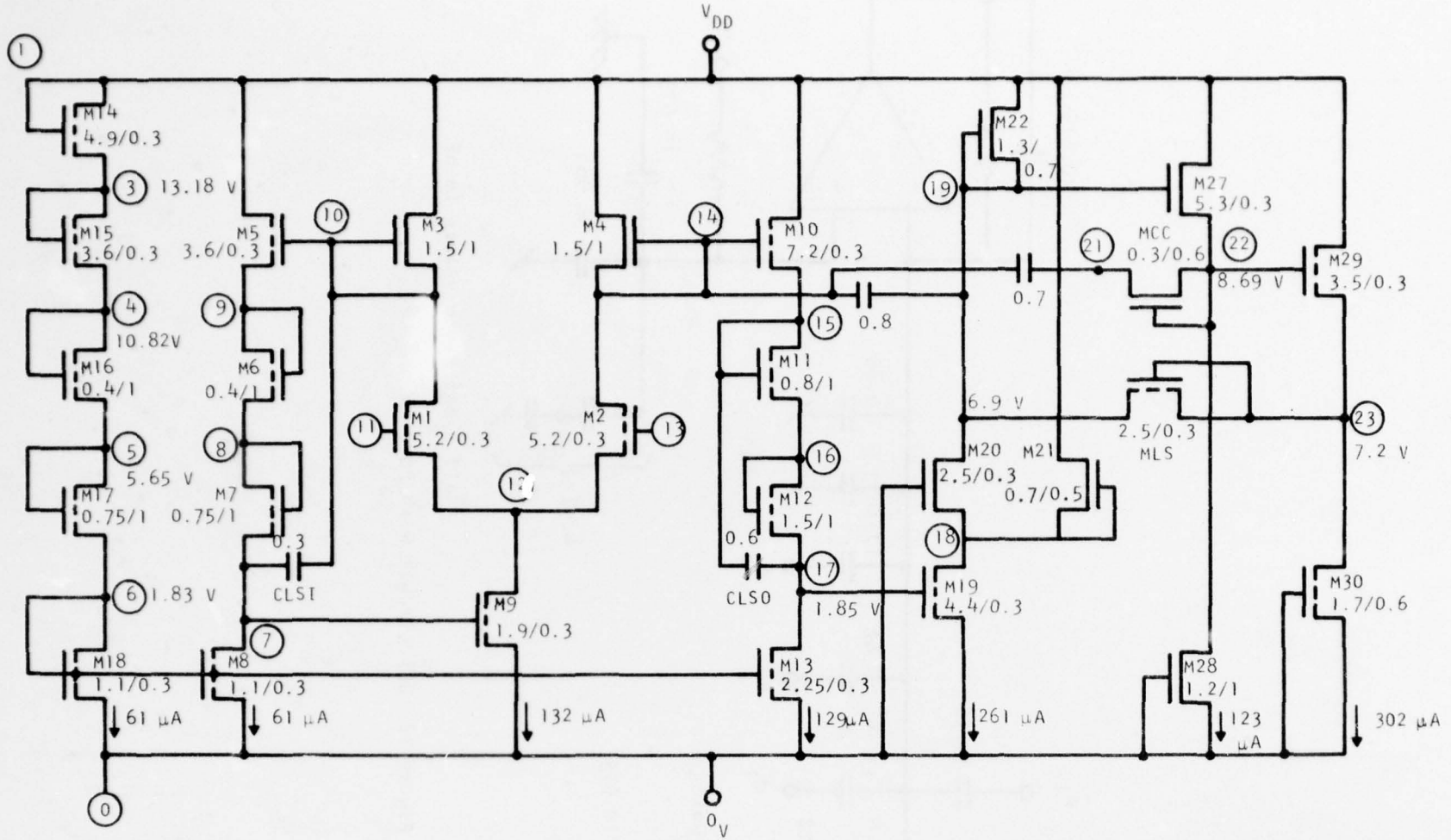


Figure 13 DCI Amplifier Schematic

The open loop transfer function of the DCI amplifier is given in the SPICE simulation output of Figure 14. The unity gain crossover frequency is 31 MHz, and the zero phase margin frequency is 18 MHz. A transient simulation for +/- 4 V output steps is illustrated in Figure 15. All steps settle to eight bits in less than 300 ns. The performance of the amplifier is summarized in Table 2.

G. Correlator Clocking

Figure 16 shows the relative timing of the ten clocks required to operate the binary/analog correlator. ϕ_A, ϕ_B, and ϕ_C are used to control the operation of the digital shift register, which in turn controls the ϕ_2 CCD clock, as discussed in Section II.C. ϕ_1', ϕ_2', and IPG control the transfer of charge between CCD registers (see Section II.E). ϕ_1 is the remaining CCD clock, ϕ_{R1} and ϕ_{R2} are the DCI reset clocks; ϕ_B and ϕ_C are also used to reset the CVAMPs. The clock timing has been designed to allow the maximum possible settling time for the DCIs and charge amplifiers. At a clock rate of 1 MHz these times are ~ 375 ns.

The clock driver circuit is shown in Figure 17. The six devices driven by the input lines act as buffers between the large gates of the output devices and the input signal drivers. They also provide an appropriate delay so that the bottom of the bootstrap capacitor MB is held at ground as an ON signal is applied. After a short delay, M2 is turned off. The source of M1 is bootstrapped to ~ 1.5 V_{DD}, and the load voltage can rise to within a threshold of V_{DD}. The device aspect ratios are determined by the required risetime and load capacitance. From the layout of the CCD and digital shift register cells, the various clock loading capacitances have been calculated and are given in Table 3. The high load capacitances result in the drive circuits occupying a considerable portion of the bar area, ~ 20%. The area of the drive circuits, designed to drive the various load capacitances with a 20 ns rise time, are also included in Table 3.

```
LEGEND:

A: VM(14)  FIRST STAGE OUTPUT MAGNITUDE
B: VM(19)  SECOND STAGE OUTPUT MAGNITUDE
C: VM(23)  DCI OPEN LOOP XFER FUNCTION MAGNITUDE (LOAD=15PF)
D: VP(14)  1ST STAGE PHASE
E: VP(19)  2ND STAGE PHASE
F: VP(23)  OUTPUT PHASE
    FREQ
(A)-------  1.000D-02  1.000D-01     1.000D+00     1.000D+01     1.000D+02
            - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(BC)------  1.000D-01  1.000D+00     1.000D+01     1.000D+02     1.000D+03
            - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(DEF)-----  -1.800D+02 -9.000D+01     0.0           9.000D+01     1.800D+02
            - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
 1.000D+05   .              .  D          .              A 2   CB       .
 1.259D+05   .              .  D          .            A . 2 CB         .
 1.585D+05   .              . D           .           A  .2 CB          .
 1.995D+05   .              . D           .          A    .22           .
 2.512D+05   .              .  D          .        A      C3            .
 3.162D+05   .              .  D          .       A      CB2            .
 3.981D+05   .              .  D          .     A      2 FE             .
 5.012D+05   .              .   D         .   A      CB  FE             .
 6.310D+05   .              .   D         .  A      CB   FE             .
 7.943D+05   .              .    D        . A     CB     FE             .
 1.000D+06   .              .     D       .A     CB      FE             .
 1.259D+06   .              .      D      A     2        FE             .
 1.585D+06   .              .        D   A.  CB          FE             .
 1.995D+06   .              .         D  A. CB           FE             .
 2.512D+06   .              .           D A.CB          F.E             .
 3.162D+06   .              .           DA2             F.E             .
 3.981D+06   .              .           C3.             F.E             .
 5.012D+06   .              .          CBAD           F  .E             .
 6.310D+06   .              .          CB A.D        F   .E             .
 7.943D+06   .              .         CB   AD       F    E             .
 1.000D+07   .              .        C B   A D     F     E.             .
 1.259D+07   .              .       C B    .AD   F       F .            .
 1.585D+07   .              .      C B     .D2         E  .            .
 1.995D+07   .              .    C  B   F D  A      E    .             .
 2.512D+07   .              .  C   2     D.  A  E        .             .
 3.162D+07   .             C F   B   D   . F A           .             .
 3.981D+07   .          2  .    B D     E.   A           .             .
 5.012D+07   .     FC      .  BD   E     .  A            .             .
 6.310D+07   . FC          .2  E         .A             .             .
 7.943D+07  C.            2 .F          A.             .            F .
 1.000D+08  C.        B D E.          A   .             .           F  .
            - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

Figure 14 DCI Open Loop Transfer Function

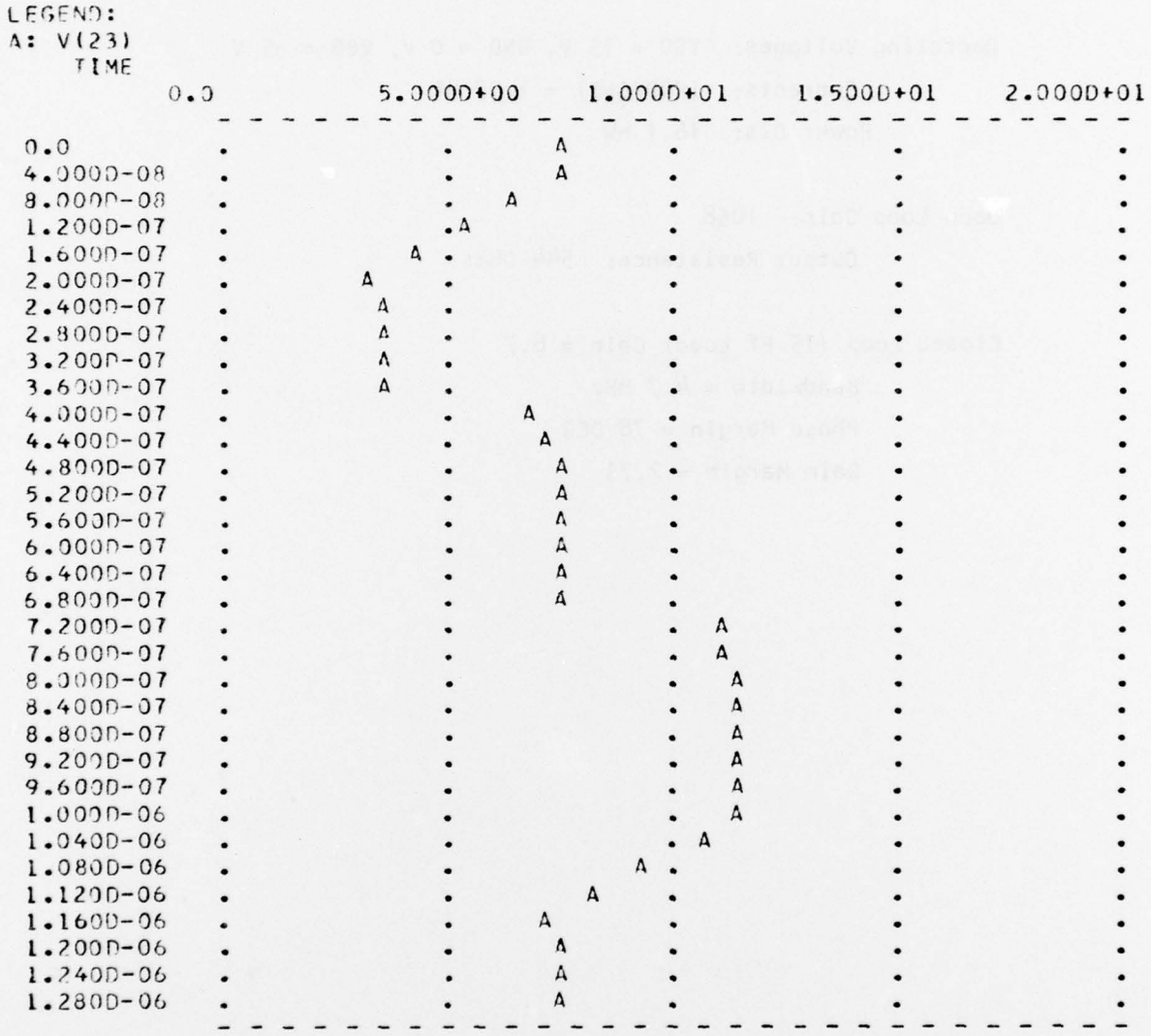


Figure 15 DCI Step Response for +/- 4 V Output Swing

Table 2

DCI Amplifier Performance

Operating Voltages: VDD = 15 V, GND = 0 V, VBB = -5 V

Currents: (FDD/GND) = 1.07 MA

Power Dis: 16.1 MW

Open Loop Gain: 1058

Output Resistance: 544 Ohms

Closed Loop (15 Pf Load) Gain = 6.7

Bandwidth = 4.7 MHz

Phase Margin = 78 DEG

Gain Margin = 2.73

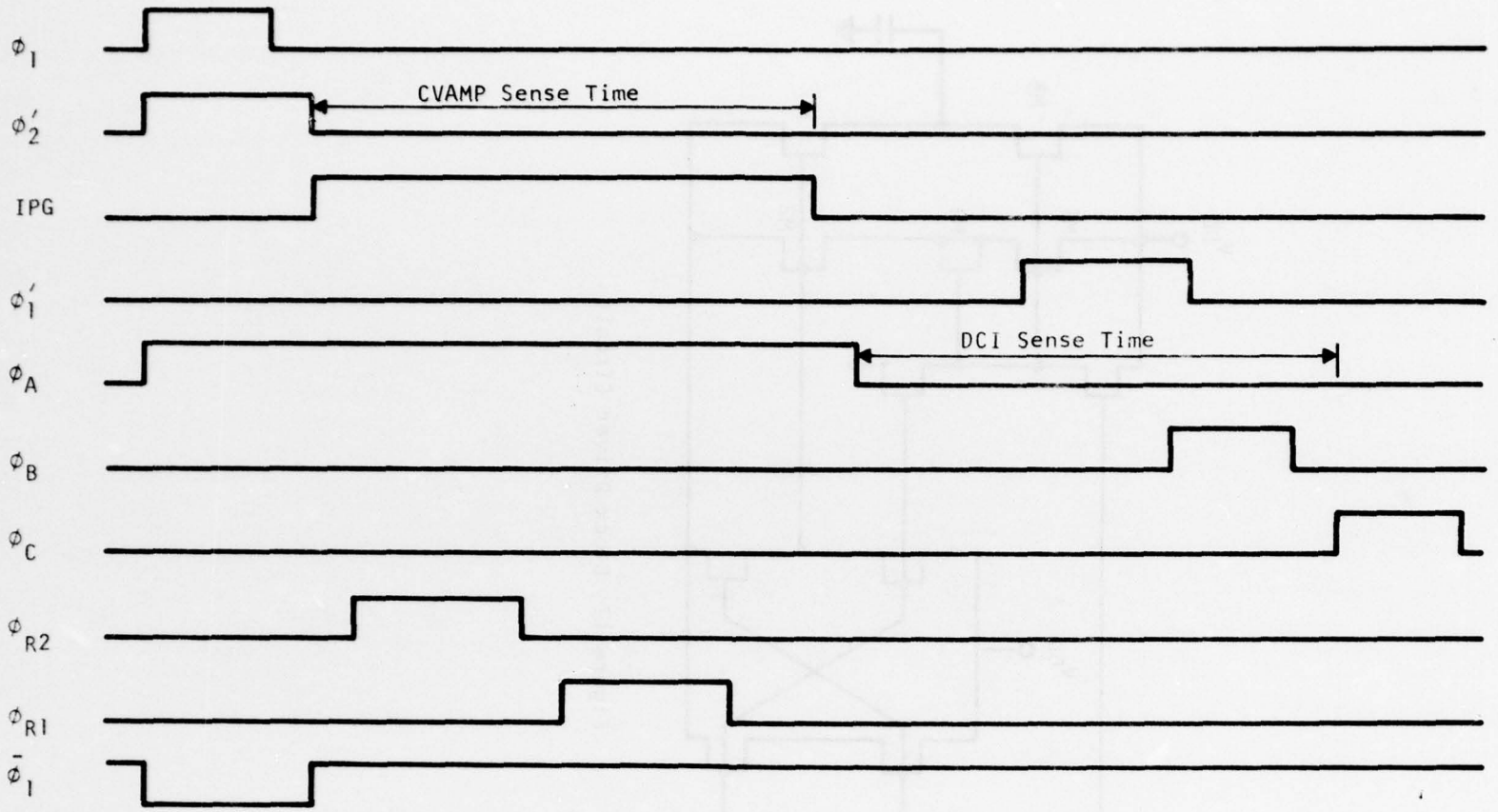


Figure 16 Correlator Clock Timing

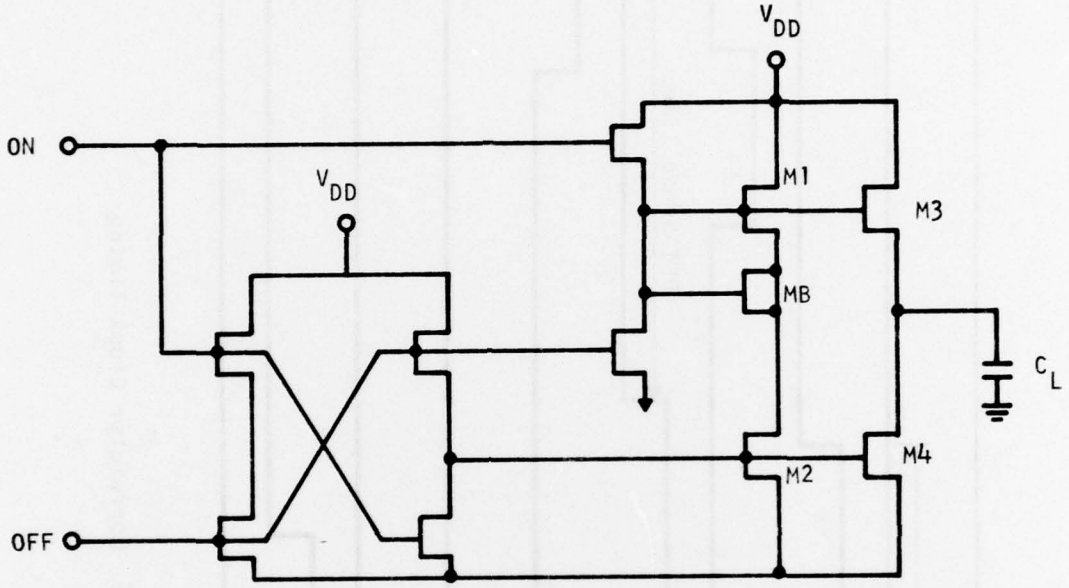


Figure 17 Clock Driver Circuit

Table 3

Loading Capacitances and Corresponding Clock Driver Areas for 20 ns Rise Time

Clock Phase	Capacitive Loading	Driver Area, $mils^2$
ϕ_1	425 pF	400
ϕ_2'	10 pF	57
IPG	7 pF	57
ϕ_1'	7 pF	57
ϕ_A	720 pF	840
ϕ_B	140 pF	213
ϕ_C	60 pF	127
ϕ_{R2}	10 pF	57
ϕ_{R1}	10 pF	57
$\bar{\phi}_1$	10 pF	57

The maximum frequency of device operation is primarily determined by the power dissipation of the drivers. The frequency limit turns out to be about 1 MHz, as with 80% efficient drivers and a 15 V clock swing, the power dissipation is $\sim$ 400 mW. To estimate the total chip dissipation, the driver dissipation must be added to that of the circuitry for generating the clock waveforms, $\sim$ 150 mW; the seven DCIs, $\sim$ 140 mW; and the 16 charge amplifiers, $\sim$ 100 mW: a total of $\sim$ 800 mW. In addition to the power dissipation restricting the maximum frequency of operation to $\sim$ 1 MHz, neither the DCIs nor the CVAMPs will settle quickly enough to permit operation at much beyond this frequency.

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Printed by
United States Air Force
Hanscom AFB, Mass. 01731